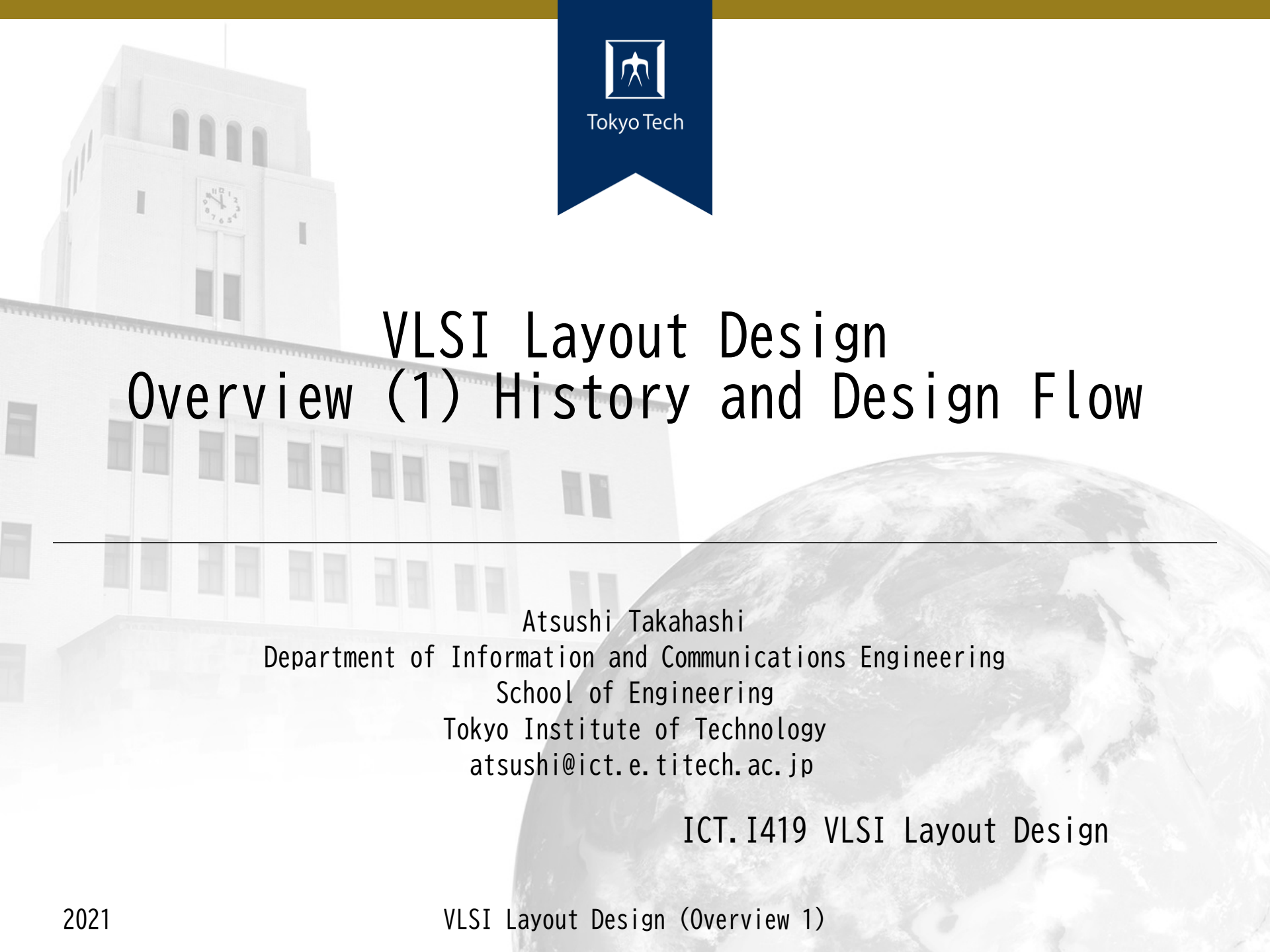

VLSI Layout Design
Overview (1) History and Design Flow

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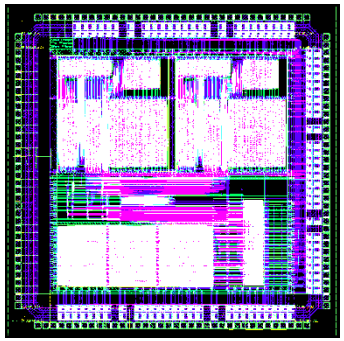
ICT.I419 VLSI Layout Design

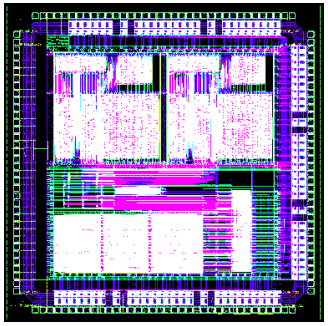
VLSI

- Very Large Scale Integrated Circuit
- Contained in a variety of products
  - Computer
    - CPU, Network
  - Consumer electronics
    - Digital TV, DVD, Mobile phone, iPad, …
  - Automotive
    - Navigation, Engine Control, …
    - Autonomous Driving
  - Others



History of VLSI

- 1959
  - Transistors, diffusive resistances, wires are fabricated on a silicon substrate by using lithography and etching technology
  - Few elements are in one chip
  - Robert Noyce (A founder of Intel)
  - Jack Kilby (Nobel Prize in Physics, 2000)

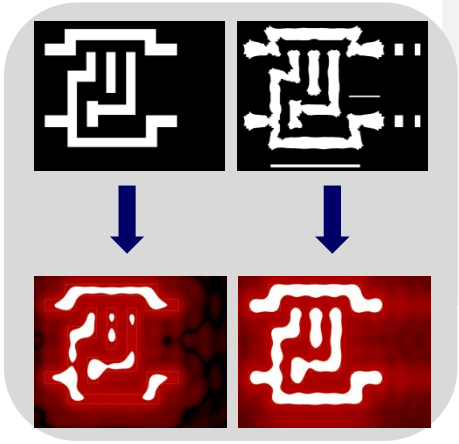


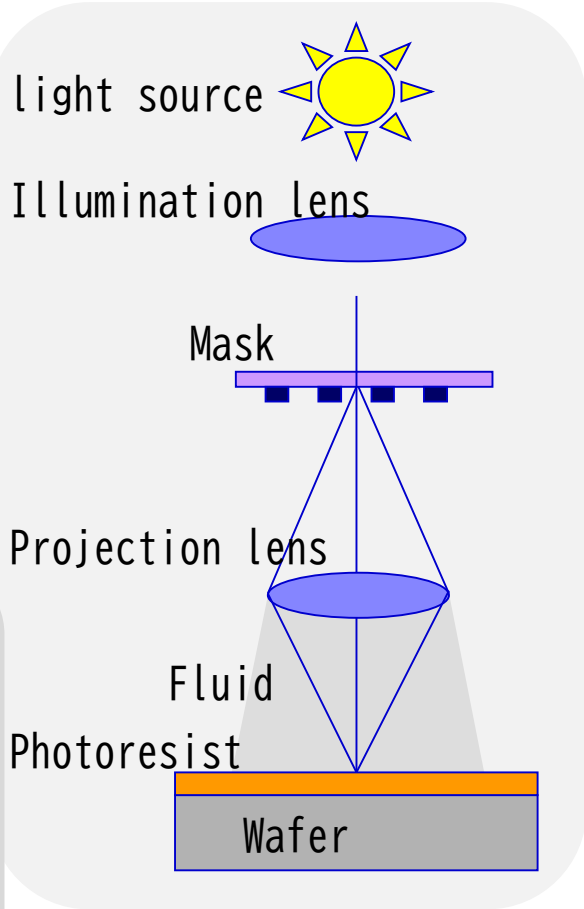
- Moore's Law: #elements in one chip
  - Twice in 1.5 year (+58% per year)
  - Now : More than 1G elements in one chip
- Makimoto's Wave
  - Alternate standardization and customization in 10 year cycles

VLSI Design / Manufacturing

Integration of Various Technologies

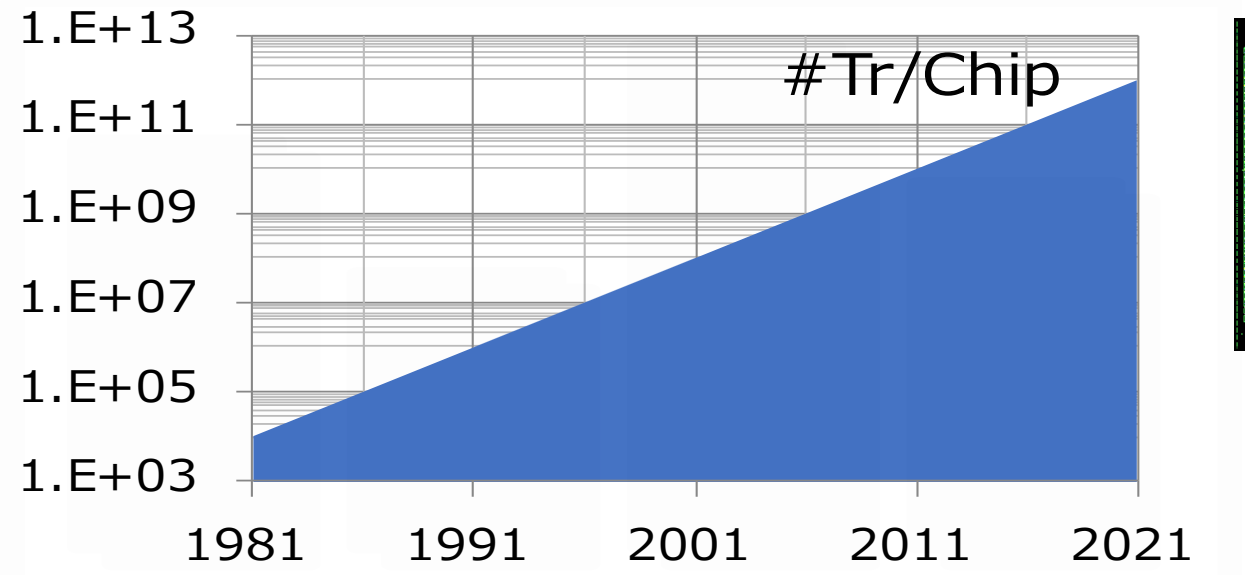
- Device Manufacture
  - Make transistors small
  - Mask Design, Exposure, Polishing, Dicing
- Circuit Design, Layout Design
  - High Speed, Low Power, Reliability
- Packaging, Printed Circuit Board
  - Wire Bonding
- System Design
- Software Design
- Marketing

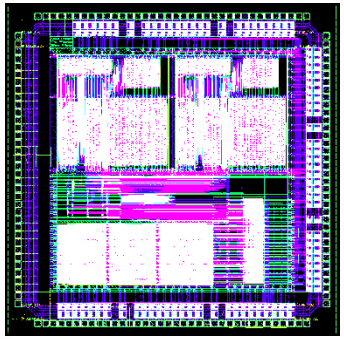




Moore's law (1965)

- Gordon E. Moore (A founder of Intel)
  - #Tr/Chip doubling every 18 months (or two years)





Typical Process: 1.2 μm, 800 nm, 500 nm, 350 nm, 250 nm, 180 nm, 130 nm, 90 nm, 65 nm, 45 nm, 36 nm, 22 nm, 12 nm

Visible light ↔ ArF laser EUV (Extremely Ultra Violet)

750–380 nm 193 nm 13.5 nm

Inevitable Paradigm Shifts

- The number of transistors in one chip becomes 100 times in every 10 years
- The smaller the feature size of VLSI chip is
  - the higher the performance of VLSI is
  - the larger the difficulty in VLSI design is

- Time-to-market constraint
- Performance (area, speed, power...) constraint

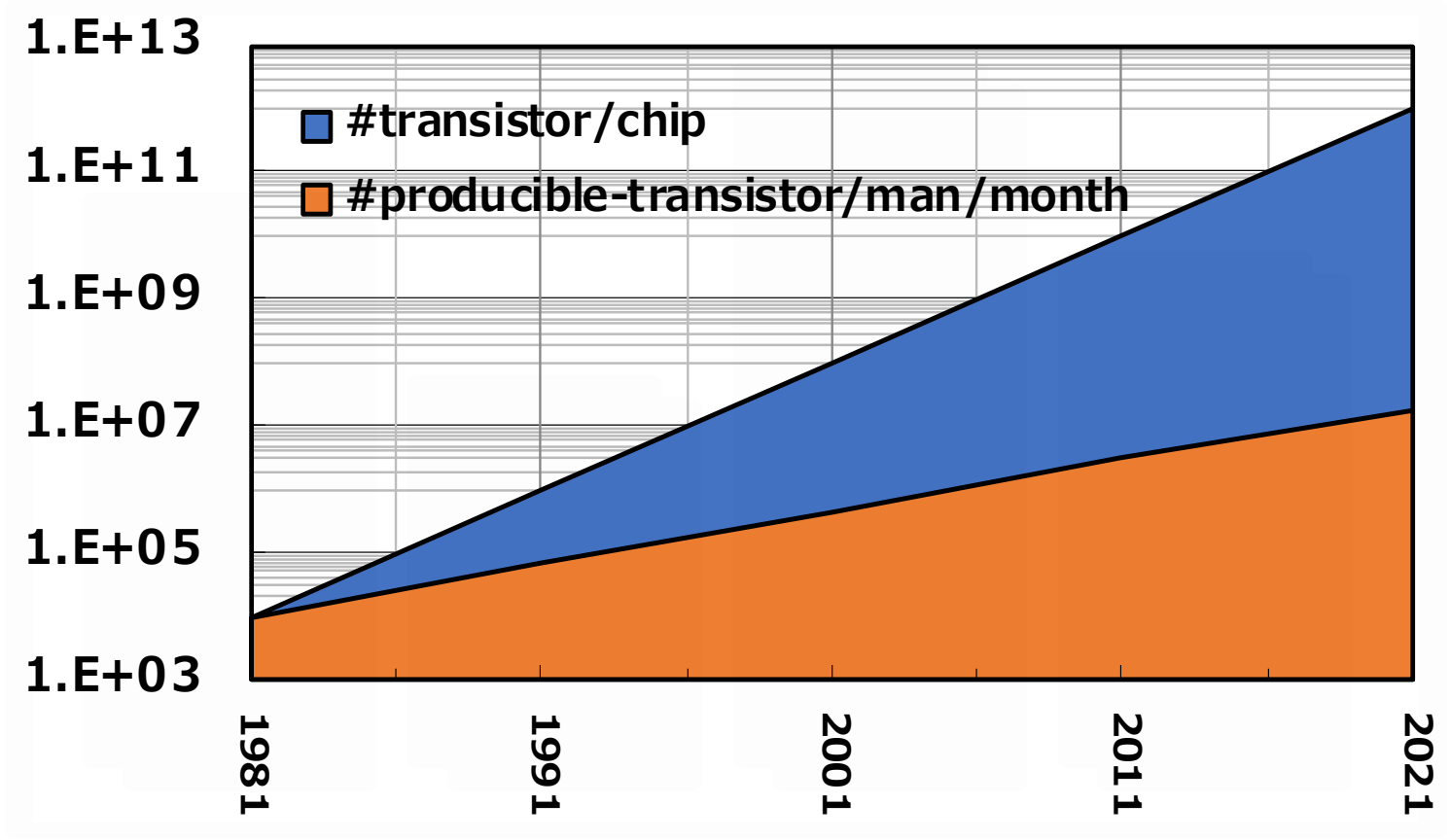
Change of Names

- IC: Integrated Circuit (1960-)
- LSI: Large Scale IC (1970-)
- VLSI: Very Large Scale IC (1980-)
- ULSI: Ultra Large Scale IC (1990-)

- System LSI
- SoC (System on Chip)
- SiP (System in Package),…

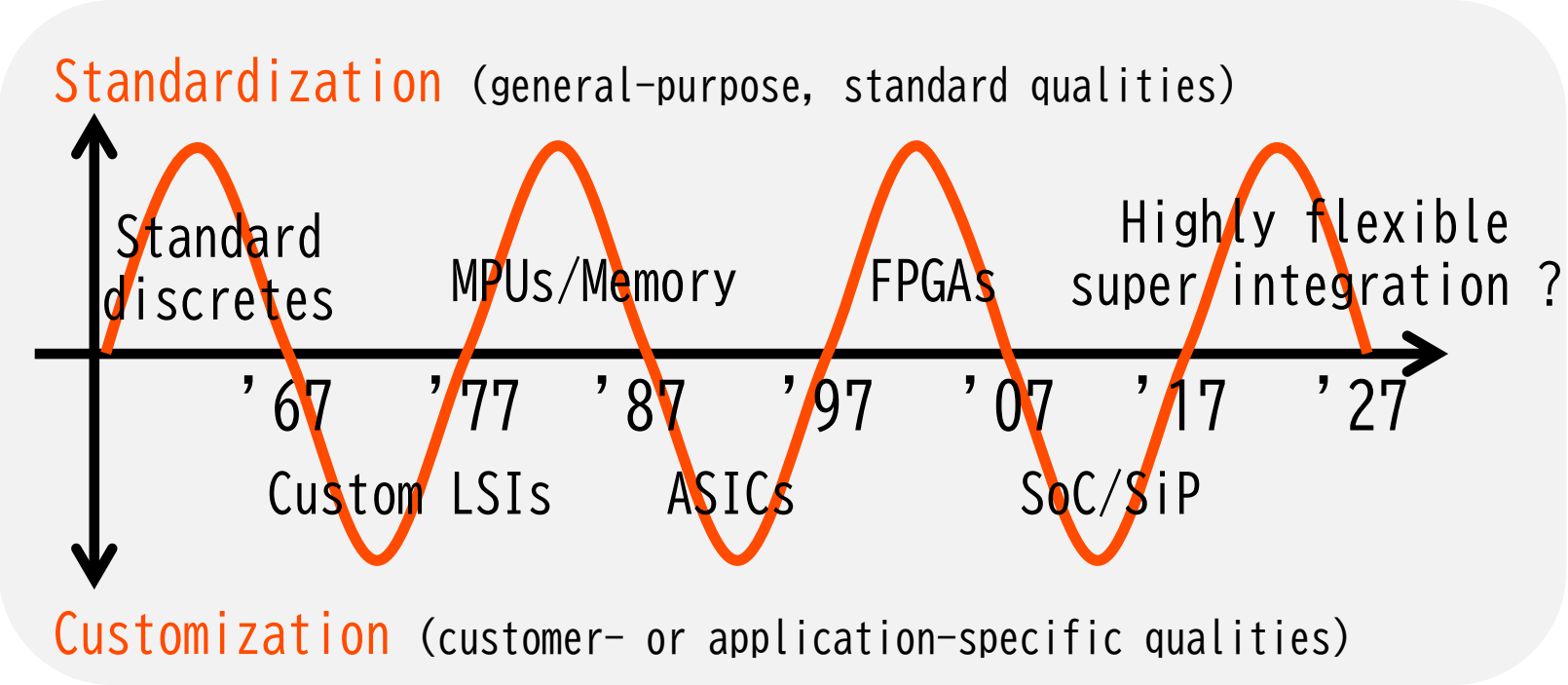
VLSI Manufacture vs. Design

- #transistor in VLSI chip +58%/year
- VLSI design productivity +21%/year



Makimoto's Wave (1987)

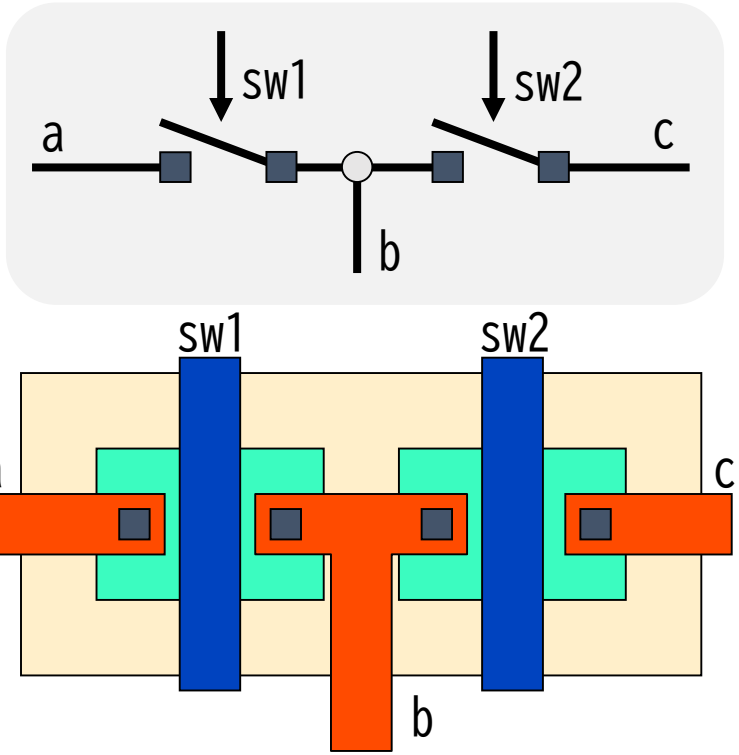
- Tsugio Makimoto (former Sony CTO etc.)
  - Semiconductor industry's cyclical alternation between standardization and customization



(COMPUTER, the IEEE Computer Society 2013)

Change of Design Method

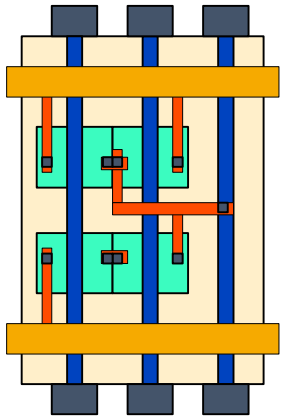
- Design Method
  - Manual Design
    - Circuit Diagram, Mask
  - Computer Aided Design
    - Boring simple tasks
  - Design Automation
    - Inferior quality but used since a circuit is too big to design manually



- Design Objectives
  - Area (Request from manufacturing, Yield, Cost)
  - Speed (Request from market, Emergence of PC)
  - Power (Emergence of Mobile products)
  - Noise (Influence to TV, Medical products)

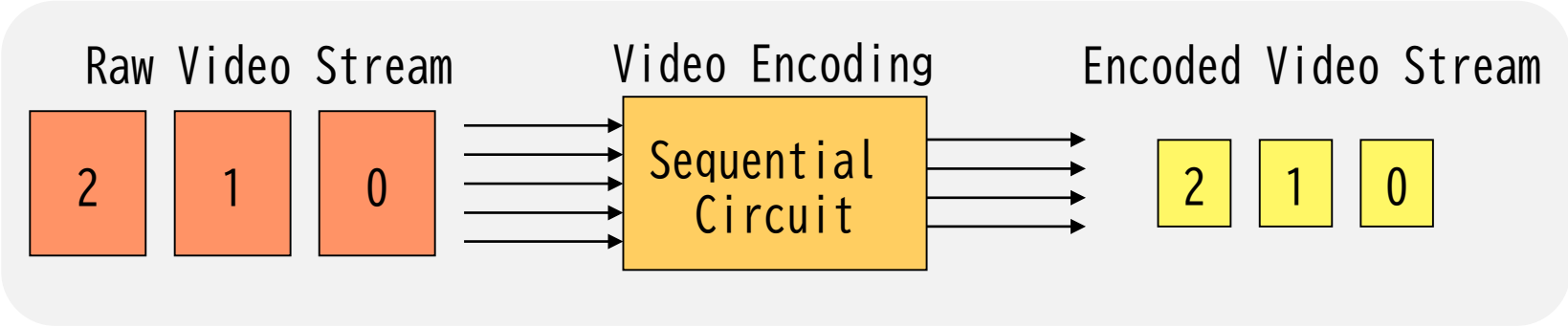
Change of Design Style

- Full Custom Design
- Semi Custom Design
- Standard Cell
  - Same cell height
- Gate Array
  - Same transistor layout
- FPGA (Field Programmable Gate Array)
  - Same logic elements
- Reconfigurable
- IP base



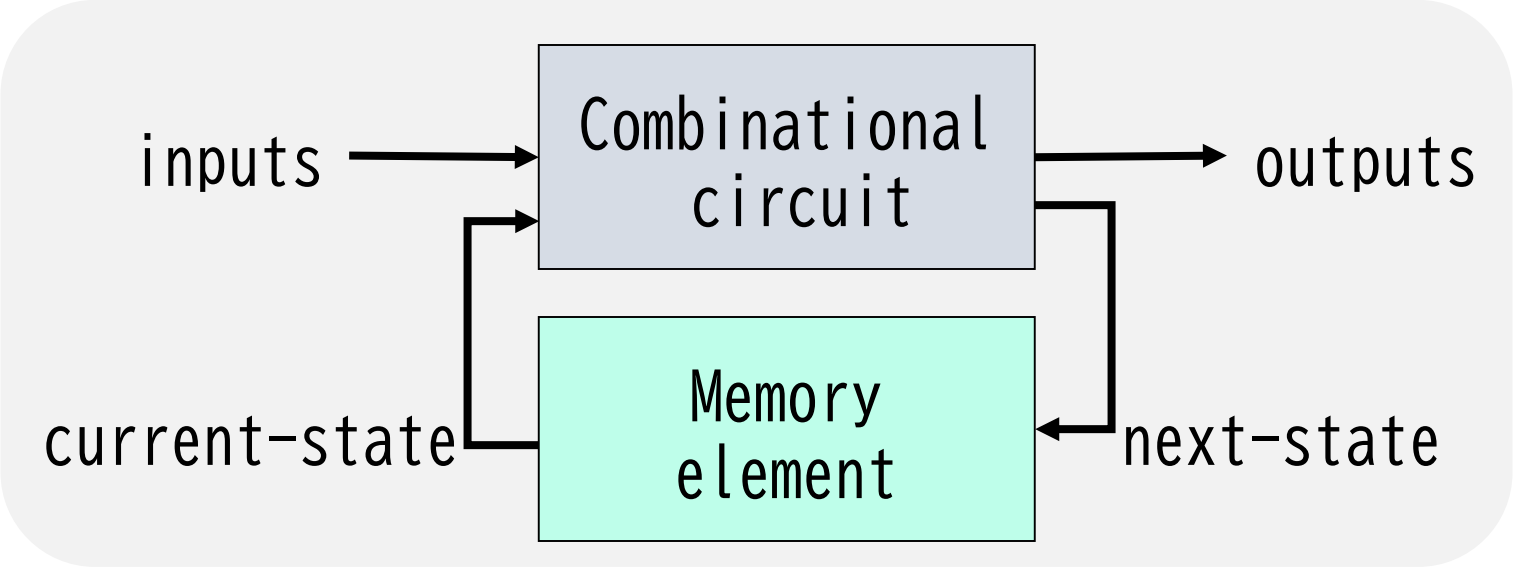
Sequential Circuit

- Inputs are given sequentially
- Input history is stored in circuit
- Outputs are generated sequentially by using inputs and stored data (history, state)



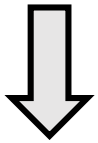
VLSI Design

- Objective: optimize
  - Area, Speed, Power, Noise, …
  - Transition time from one state to another
    - Correct output must be recognized
    - Correct state must be stored



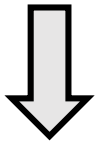
Typical Design Flow

Behavioral specification (C, VHDL, data flow graph, etc.)



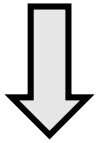
high-level synthesis

RTL description (registers, modules, MUX, etc.)



logic synthesis

Gate level circuit (NAND, NOR, etc.)

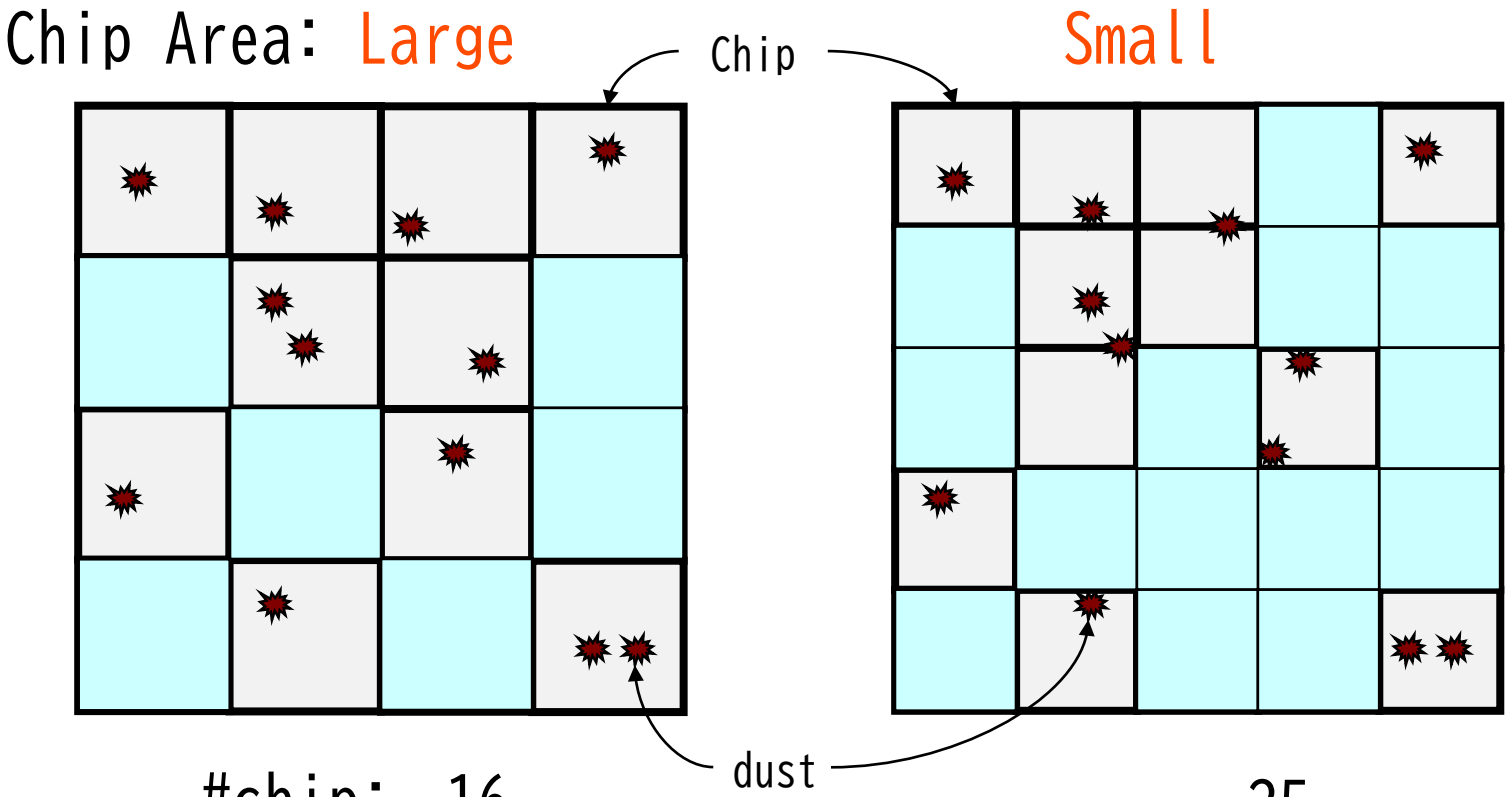


physical (layout) synthesis

Layout

Desire for Chip Area Reduction

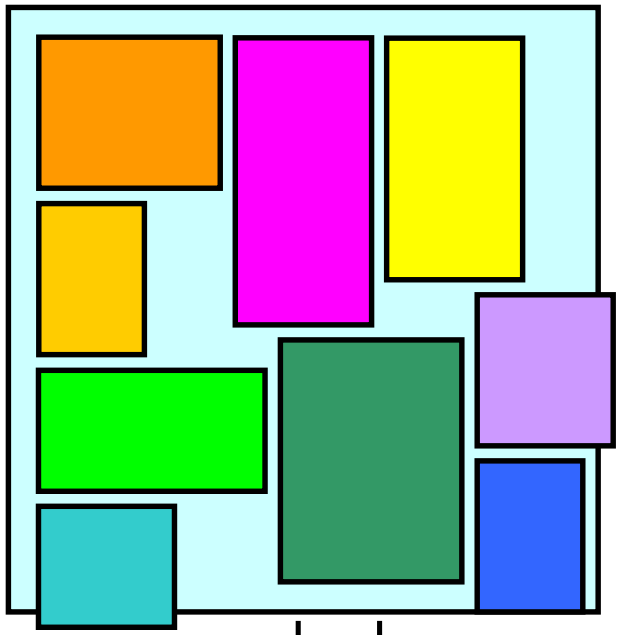
- More chips and more earnings
  - ✓Cost per wafer is almost constant



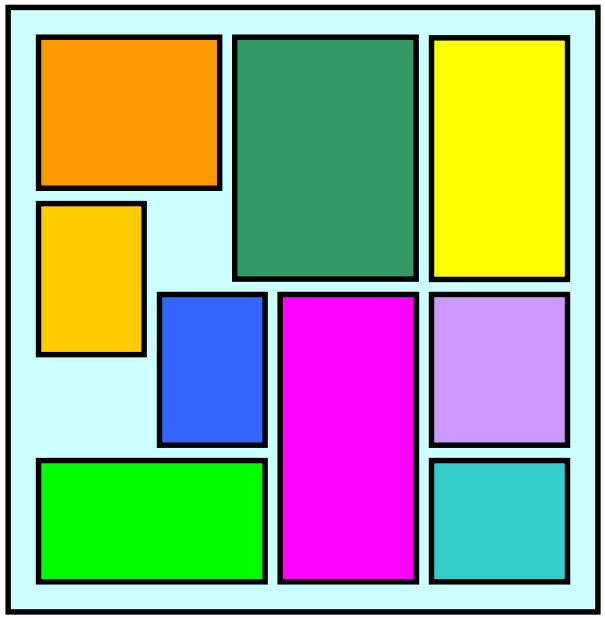
Packing Problem

- Not so difficult if the number of modules is small
  - An optimal solution can not be found in practical time in general if the number of modules is large

✓ In VLSI design, routing should be taken into account



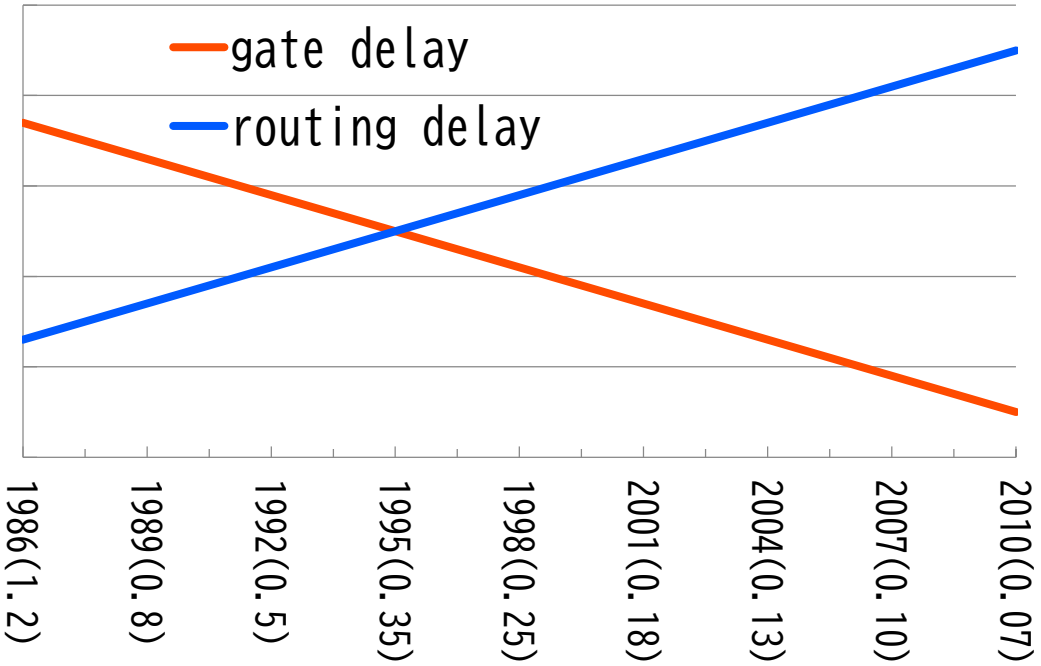
bad

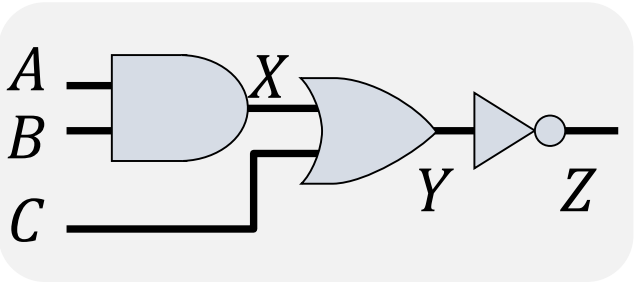


good

Design rule vs. Typical delay

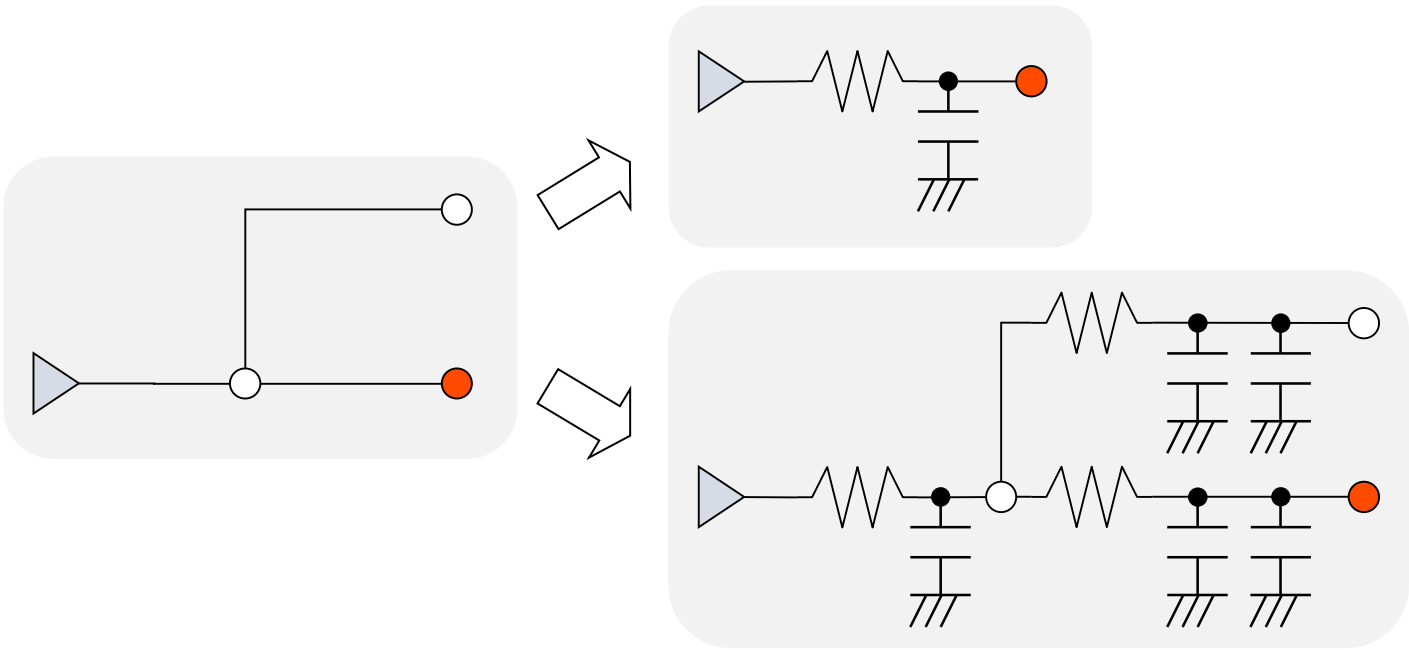
- Feature size becomes small, then
  - transistor switching speed increases
  - wire resistance increases





Delay Model Evolution

- Previous: routing delay = length
- Current: routing delay = length + distance
- Future: more accurate model is necessary

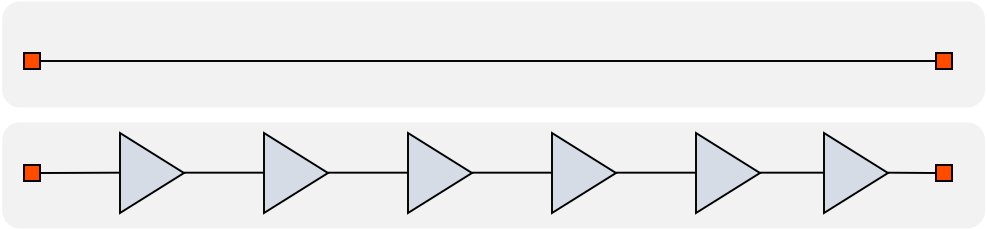


Growth of Layout Importance

- Signal Delay Estimation
  - Previous: gate level consideration is enough
    - signal delay is proportional to #gate

    routing hardly affect signal delay
  - Future: layout consideration is essential
    - signal delay depends on its path

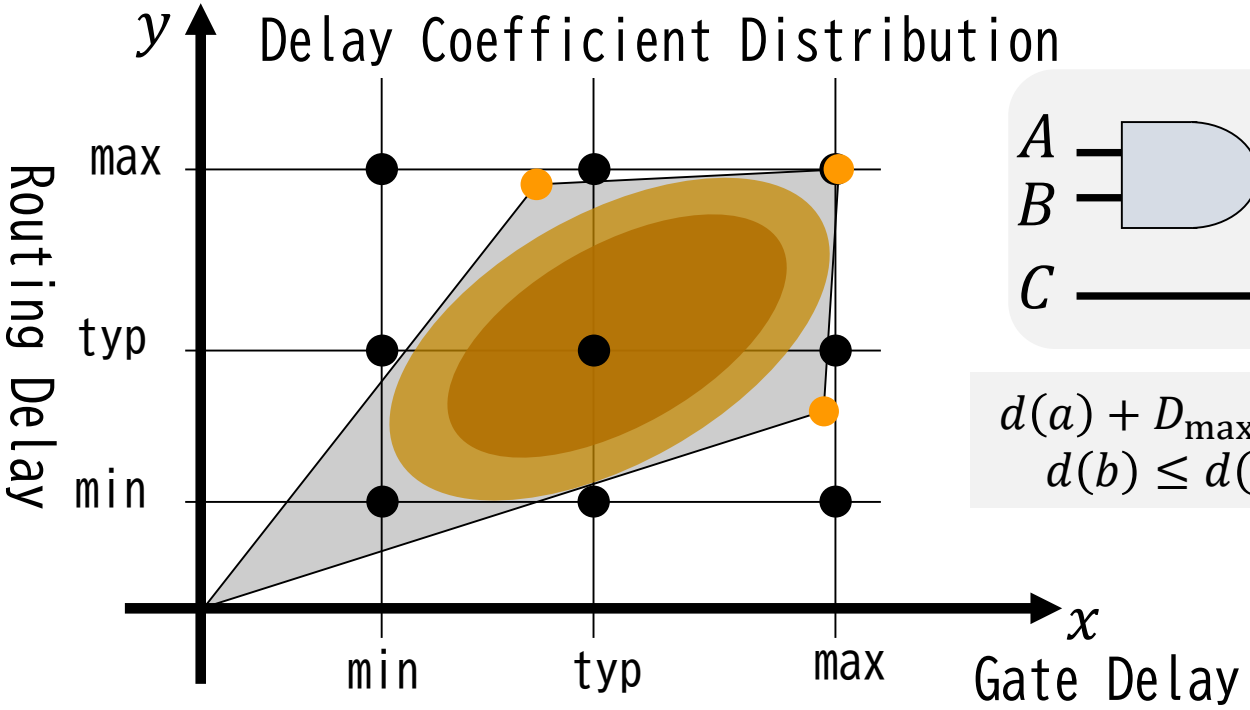
    existence of gate hardly affect signal delay

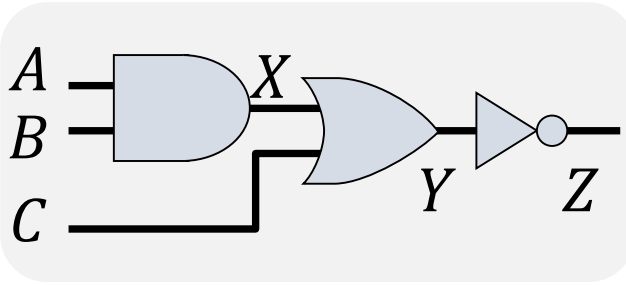


same delay?

Global Delay Variation

- Routing Delay and Gate Delay change independently
  - ✓ $D_{\text{total}} = x \times D_{\text{gate}} + y \times D_{\text{wire}}$
    - Verification in 9 Conditions (Safety, Pessimistic)
    - 3 conditions are enough (Theoretically)

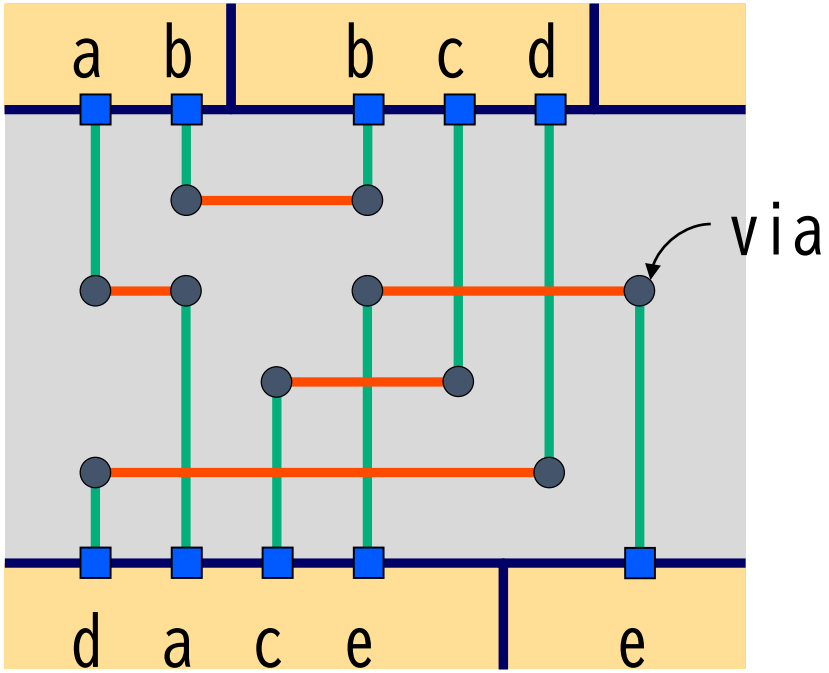




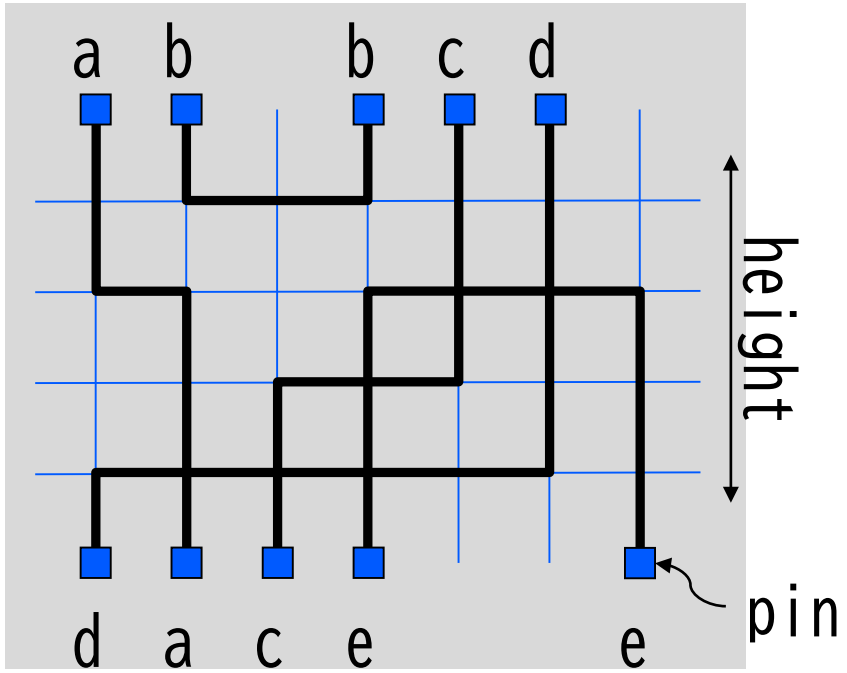
$$d(a) + D_{\max}(a,b) \leq T + d(b)$$
$$d(b) \leq d(a) + D_{\min}(a,b)$$

Channel Routing

- 2-Layer Channel Routing
  - Connect pins on the boundary of routing area using 2-layer
  - Minimize the number of tracks (height, width) of channel

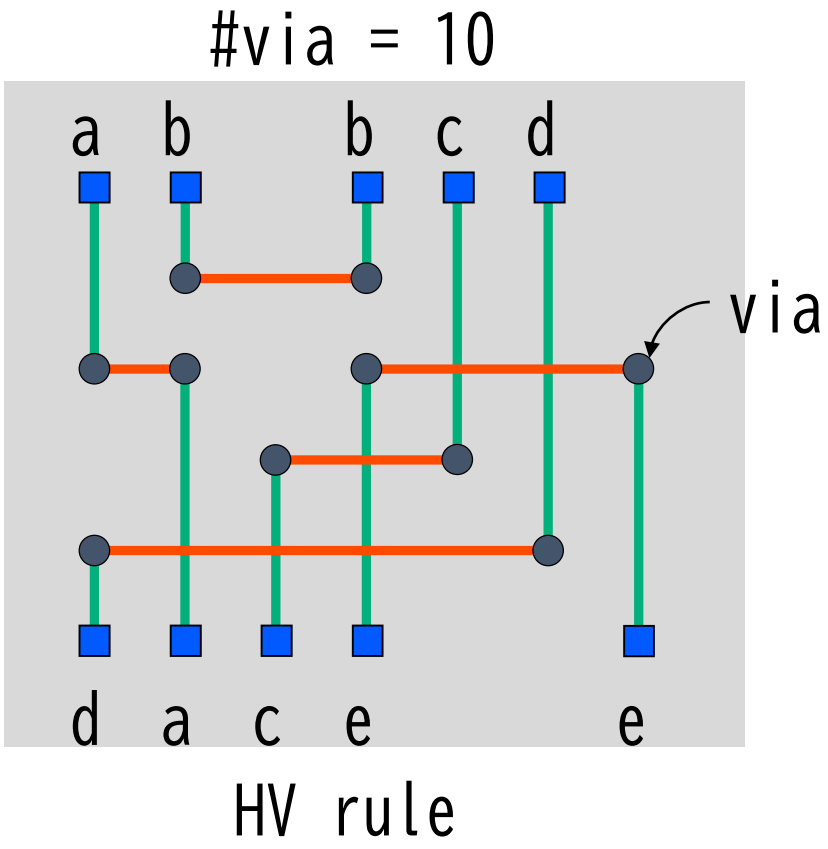


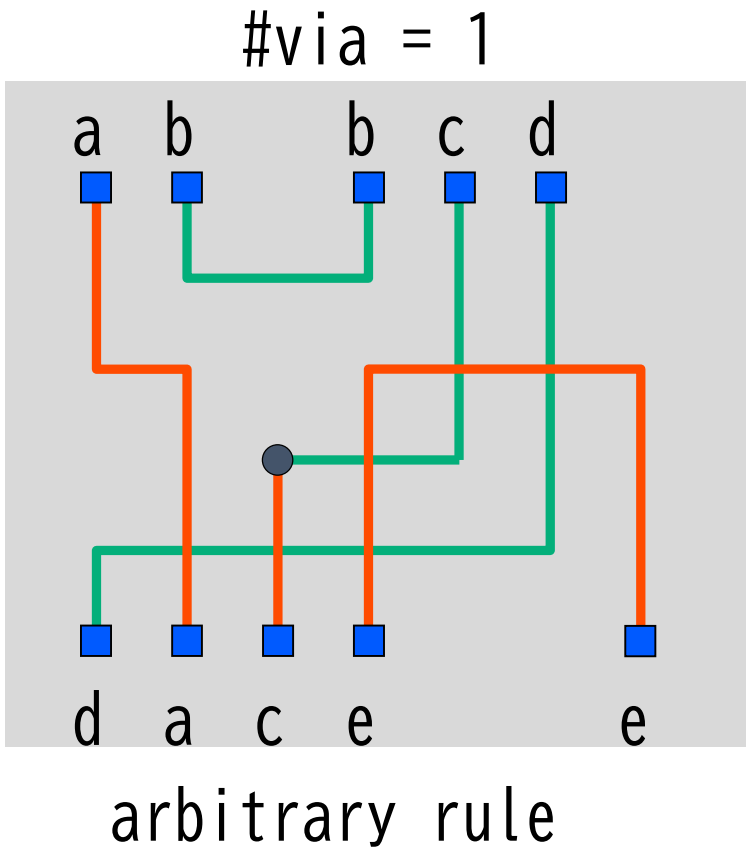
HV rule



Via Problem

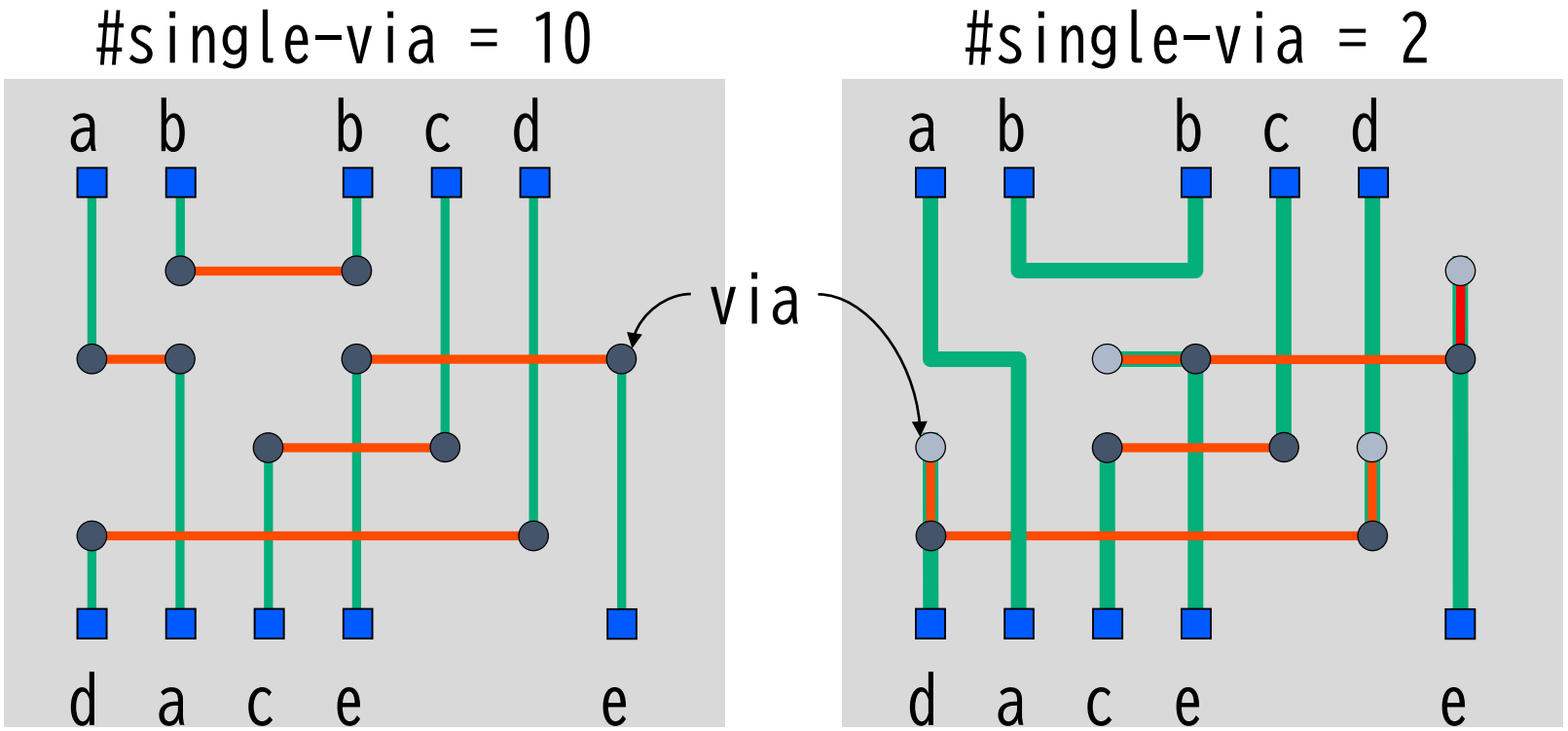
- Via Minimization
  - Minimize #via by assigning wires into proper layer



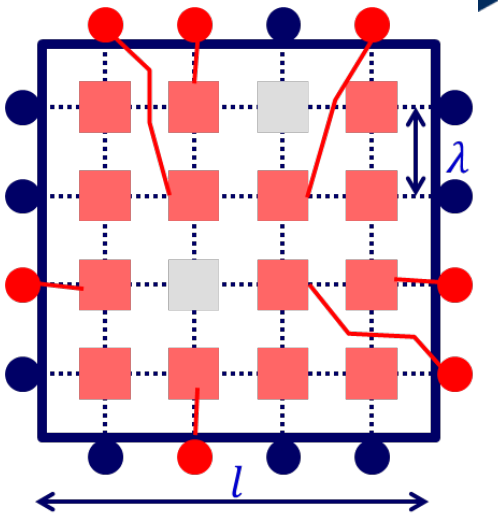


Via Problem (2)

- Double Via Insertion
  - Minimize #single-via to improve the reliability



Pin Crisis



- Assumption 1
  - Chip is a square with length l
  - Chip area $S = l^2$
  - Grid interval λ
    - minimum feature size
    - minimum spacing
    - precision of lithography
  - The amount of functionality on chip $Q = \alpha \frac{S}{\lambda^2}$ (α : constant)
- Assumption 2
  - The number of required pins $P_{req} = \frac{Q}{\beta}$ (β : constant)
    - 1 pin is needed for every β pins
- Assumption 3
  - The number of available pins $P_{sup} \leq \frac{4l}{\lambda}$

An upper bound of chip functionality

- The maximum functionality is independent of λ
  - $P_{req} = \frac{Q}{\beta}$, $P_{sup} \leq \frac{4l}{\lambda}$, $Q = \alpha \frac{S}{\lambda^2}$

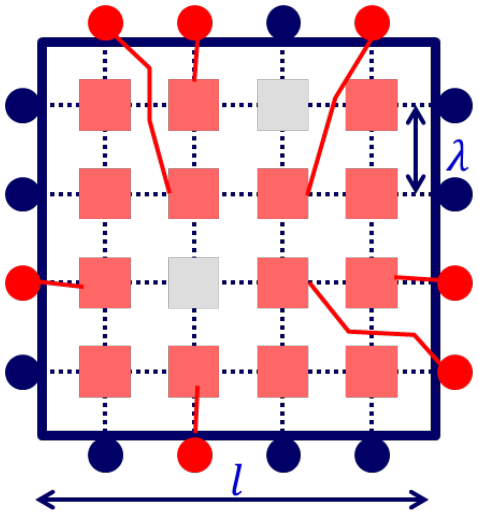
$$P_{req} \leq P_{sup}$$

$$\Rightarrow \quad \frac{Q}{\beta} \leq \frac{4l}{\lambda}$$

$$\Rightarrow \quad Q^2 \leq \beta^2 \frac{16l^2}{\lambda^2}$$

$$\Rightarrow \quad \alpha \frac{S}{\lambda^2} Q \leq \beta^2 \frac{16S}{\lambda^2}$$

$$\Rightarrow \quad Q \leq 16 \frac{\beta^2}{\alpha}$$



- Miniaturization does not always increase the functionality on chip
  - α : element density
  - β : pin demand ratio (1 pin is needed for every β pins)

Example

- $Q \leq 16\frac{\beta^2}{\alpha}$
  - $\alpha = 1, \quad \beta = 1 \quad \Rightarrow \quad Q \leq 16$
  - $\alpha = 7/8, \beta = 2 \quad \Rightarrow \quad Q \leq 73$

  - $Q = 4000 \quad \Rightarrow \quad \alpha = \frac{2}{5}, \beta = 10$
  - $Q = 40000 \quad \Rightarrow \quad \alpha = \frac{1}{25}, \beta = 10$

Problem 1.1

- If we regard placement problem as combinatorial problem, a basic placement problem would be "divide region into subregions (rooms) and assign at most one element to each subregion (room)."
  1. Assign distinct n blocks to k^2 subregions (rooms). Give the number of distinct assignments $f(k,n)$ where $k^2 \geq n$.
  2. Assign distinct n blocks to n^2 subregions (rooms). Assume that it takes 1 μs to evaluate one assignment. What is the maximum n to evaluate all distinct assignments within "*one space-time*" which is 13.8 billion years? What is the maximum n within ten space-times?

Problem 1.2

- Consider more practical assumptions in the discussion of pin crisis.
  1. Give an upper bound of chip functionality when Assumption-1 changes "Chip is a rectangle with aspect ratio γ (≥ 1)".
  2. Assumption-2 suggests that the number of connections to the outside is linearly proportional to the number of internal elements. However, Rent's law claims that $P_{req} \sim Q^{\varepsilon}$ $(0 < \varepsilon < 1)$. Give an upper bound of chip functionality according to Rent's law. Discuss it by using numerical example.
  3. Assumption-3 can be relaxed by placing I/O pins inside the chip area as well as perimeter of the chip. Give an upper bound of chip functionality when $P_{sup} = \frac{\delta l}{\lambda}$ $(\delta > 4)$.
  4. The fact that the order of area is larger than that of perimeter causes pin crisis. Discuss the effect of multi-layer and/or 3-dimensional fabrication on pin crisis.