## Problem 5

Consider the data-flow graph in Fig.5. Assume that multiplication takes 2 clock cycles and addition takes 1 clock cycle to execute.
A) Compute the scheduling based on following scheduling algorithms:

1. ASAP scheduling
2. ALAP scheduling
3. Force-directed scheduling
4. List scheduling (assume 2 multipliers and 1 adder)
(NOTE1 : for ALAP and force-directed scheduling, set $T_{\text {max }}=10$ )
(NOTE2 : for list scheduling, use mobility as the priority function)


Fig. 5 Data-Flow Graph

## Problem 5

B) Do register binding on the following binding algorithms:

1. Left-edge algorithm
2. Clique partitioning (consider the interconnect cost)
(NOTE1 : use the operation scheduling result of either force-directed scheduling or list scheduling)
(NOTE2 : schedule the input node $\mathrm{v}_{0}, \mathrm{v}_{3}, \mathrm{v}_{2}$ at $t=0$, and schedule the output nodes $\mathrm{v}_{12}, \mathrm{v}_{13}, \mathrm{v}_{14}$ at $t$ $=T_{\max }-1$ )
C) Do functional unit binding on the multiplications (consider the interconnect cost)
D) Do port binding on the adder inputs.
E) Draw the diagram of the synthesized datapath based on the above results.


Fig. 5 Data-Flow Graph

