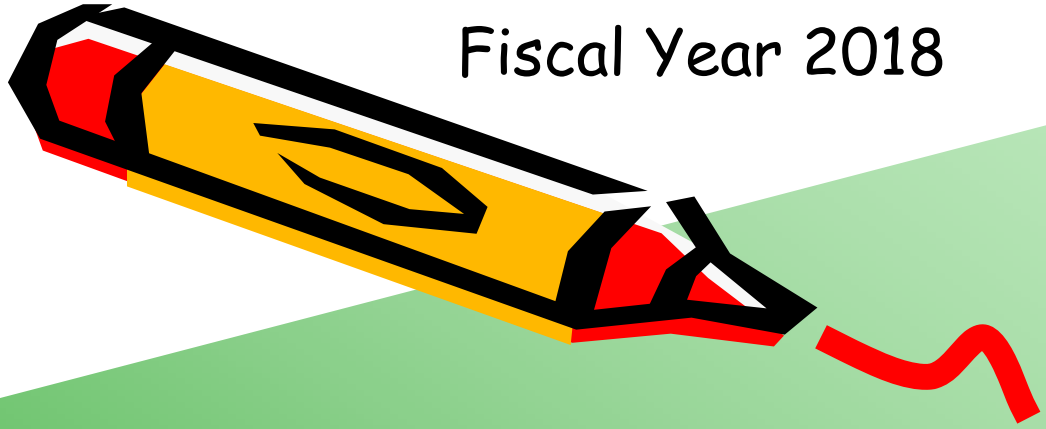
Fiscal Year 2018

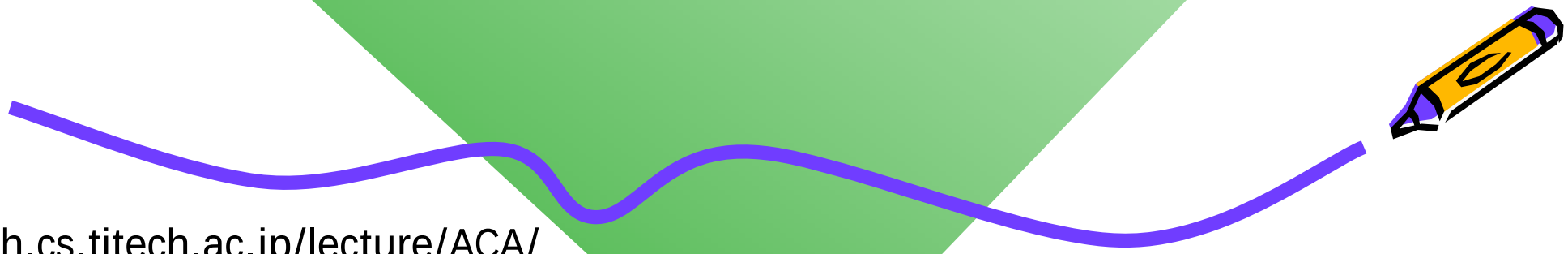
Ver. 2018-12-21a



Course number: CSC.T433
School of Computing,
Graduate major in Computer Science

Advanced Computer Architecture

Mid-term report



www.arch.cs.titech.ac.jp/lecture/ACA/
Room No.W936
Mon 13:20-14:50, Thr 13:20-14:50

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Mid-term report

1. Submit your report printed on A4 paper at the beginning of the next lecture on January 7, 2019
2. Enjoy designing the processors and prediction hardware and debugging of them.

1. MIPS assembly programming

- Write MIPS assembly code asm1.s for code1.c in C.

```
int sum = 0;
int i;
for (i=0; i=<100; i++) sum += i;
```

code1.c

- Write MIPS assembly code asm2.s for code2.c in C.

```
int A[100];
int sum = 0;
int i;
for (i=0; i<100; i++) A[i] = i;             /* initialize the array */
for (i=1; i<100; i++) A[i] = A[i-1] + A[i]; /* compute              */
for (i=0; i<100; i++) sum += A[i];          /* obtain the sum       */
```

code2.c

2. Single-cycle processor

- Design a single-cycle processor supporting MIPS add, addi, lw, sw, and bne instructions in Verilog HDL. Please download proc04.v from the support page and refer it.
- Verify the behavior of designed processor using asm1.s and asm2.s.
- The report should include a block diagram, a source code in Verilog HDL, the description of the changes of the code, and obtained waveforms of your design.

3. Pipelined processor

- Design a five stage pipelined scalar processor supporting MIPS add, addi, lw, sw, and bne instructions in Verilog HDL. Please download proc07.v from the support page and refer it.
  Note that you do not need to implement data forwarding.
- Verify the behavior of designed processor using asm1.s and asm2.s.
  You may insert NOP instructions if necessary.
- The report should include a block diagram, a source code in Verilog HDL, the description of the changes of the code, and obtained waveforms of your design.

4. Gshare branch prediction

- Implement a Gshare branch prediction on a five stage pipelined scalar processor supporting MIPS add, addi, lw, sw, and bne instructions in Verilog HDL. Please download proc08.v from the support page and refer it.
  - The prediction and the BHR update are done in IF stage, and the update of PHT is done in WB state.
  - PHT is implemented as one read and one write port memory.
  - Note that you do not need to implement data forwarding.
- Evaluate the prediction accuracy (hit ratio) of your design using the instructions in proc08.v.
  - Use the simulation until #800000 for the evaluations. You have to make about 2110 predictions.
  - Verify the number of PHT entries of Gshare and evaluate hit ratios.
- The report should include a block diagram, a source code in Verilog HDL, the description of the changes of the code, the evaluation results, and obtained waveforms of your design.