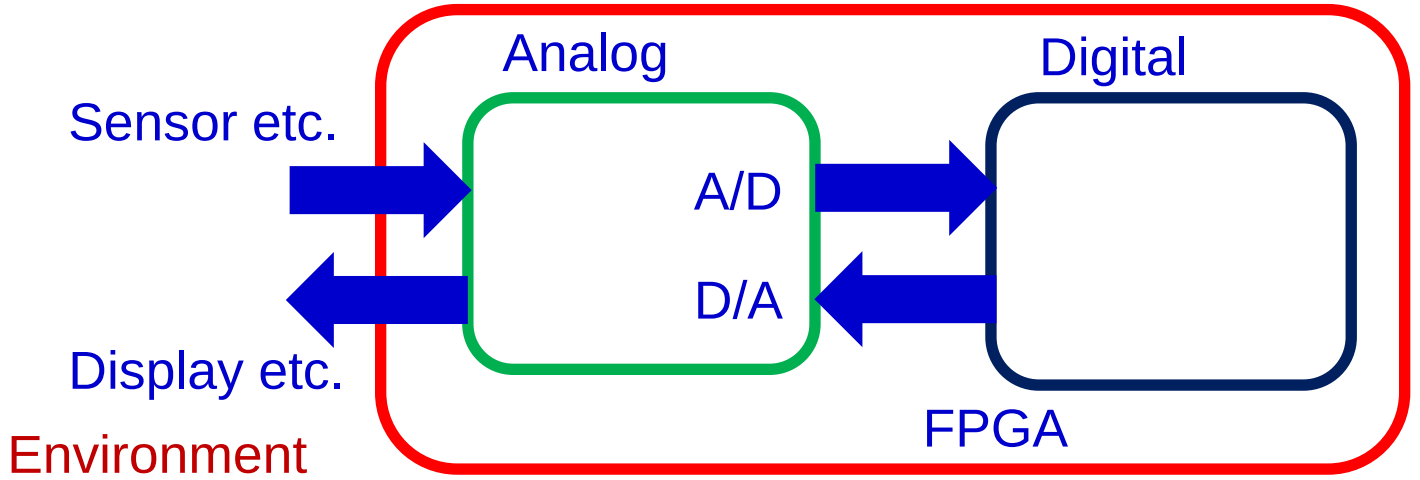
Digital Integrated Circuits 1: Fundamentals

Atsushi Takahashi
Department of Information and Communications Engineering
School of Engineering
Tokyo Institute of Technology

VLSI and Computer System

- VLSI (Very Large Scale Integrated Circuits)
- Computer System

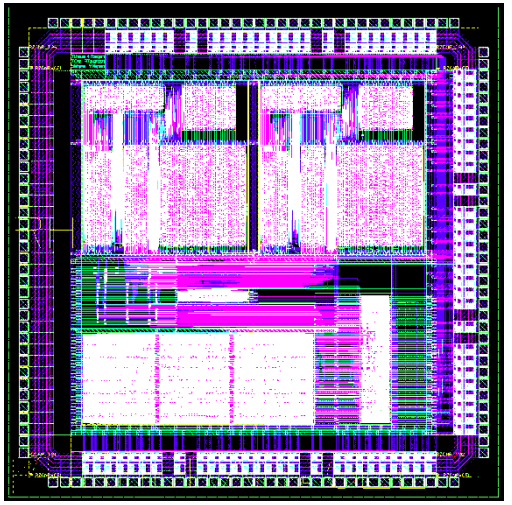


Computer System / Embedded System / VLSI …

Architecture : Microprocessor / Deep Neural Network …
Hardware : Logic Functions, Hardware Description Language …
Software : Algorithm, Real Time Operating System …
Design : Synthesis, Compiler, Physical Design …

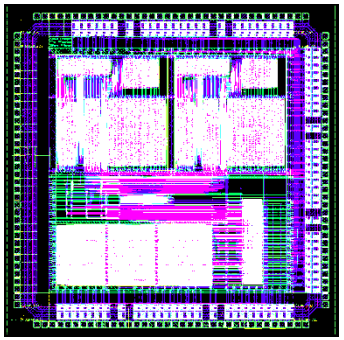
VLSI

- Very Large Scale Integrated Circuits
- Contained in a variety of products
  - Computer
    - CPU, Network
  - Consumer electronics
    - Digital TV, DVD, Mobile phone, iPad, …
  - Automotive
    - Navigation, Engine Control, …
    - Autonomous Driving
  - Others



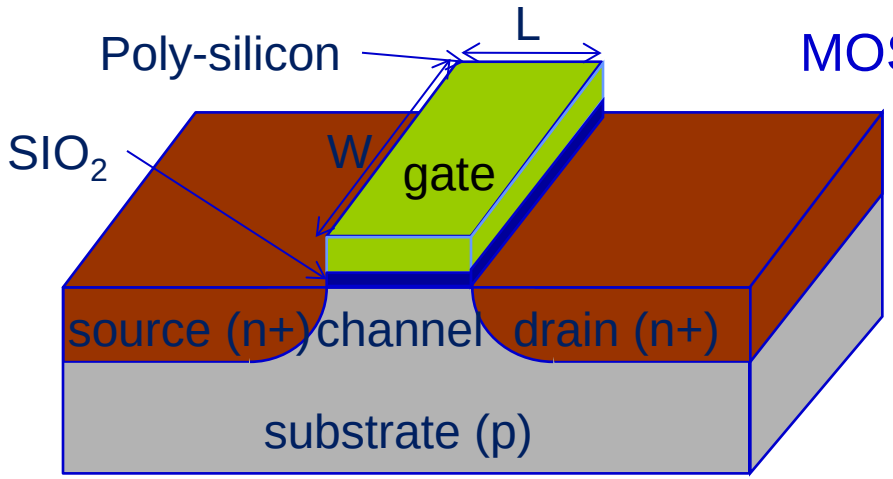
History of VLSI

- 1959
  - Transistors, diffusive resistances, wires are fabricated on a silicon substrate by using lithography and etching technology
  - Few elements are in one chip
  - **Robert Noyce** (A founder of Intel)
  - **Jack Kilby** (Nobel Prize in Physics, 2000)
- Moore's Law: #elements in one chip
  - Twice in 1.5 year (+58% per year)
  - Now : More than 1G elements in one chip
- Makimoto's Wave
  - Alternate standardization and customization in 10 year cycles



Transistor Switch

- Basic Item to control the voltage of a node
- nMOS (npn type) Transistor

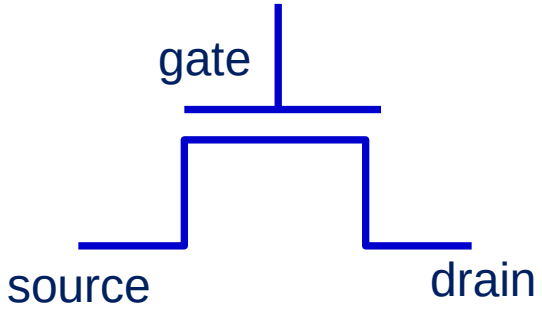


3D Image

MOSFET: MOS field-effect transistor

Metal: Poly-silicon
Oxide: SiO_2: Insulator
Semiconductor: Silicon

Top view Image



Symbol

Historical Computers in Japan

- Relay Computer, Fujitsu
  - Relay-elements from telephone exchange equipment
  - Toshio Ikeda
  - FACOM100, 1954
  - FACOM128A, 1956
  - FACOM128B, 1958
    - Commercial computer
      - Still working model was manufactured in 1959
    - IPSJ Information Processing Technology Heritage

Historical Computers in Japan

- Parametron Computer, NEC
  - SENAC-1(NEAC1102), 1958
  - First commercial computer by NEC
    - Hitoshi Watanabe
      - IEEE Kirchhoff Award 2010
        - » Filter design theory and computer-aided circuit design
    - IPSJ Information Processing Technology Heritage

Historical Computers in Japan

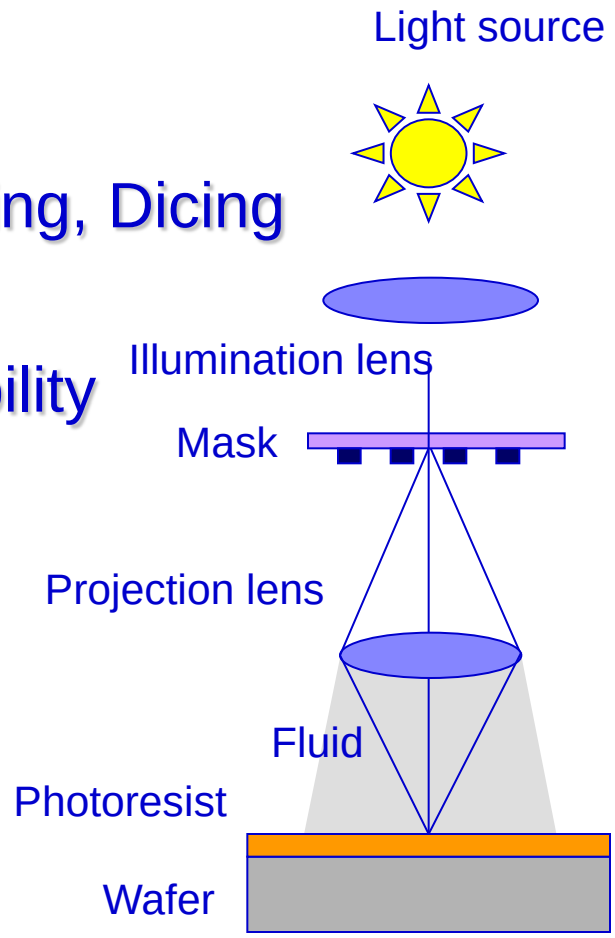
- Electronic Calculators, Sharp
  - CS-10A, 1964
    - Germanium-Transistor
      - First all-transistor diode electronic desktop calculator in the world
    - 25 kg
    - 535,000 Yen (= 1,500 US$)
      - Initial monthly salary of graduate = 21,526 Yen
      - Toyota Corolla 1100cc = 432,000 Yen (1966)

        50th Anniversary G“50 Limited” = 2,400,000 Yen (2016)
    - IEEE milestone 1964-1973
    - IPSJ Information Processing Technology Heritage

VLSI Design / Manufacturing

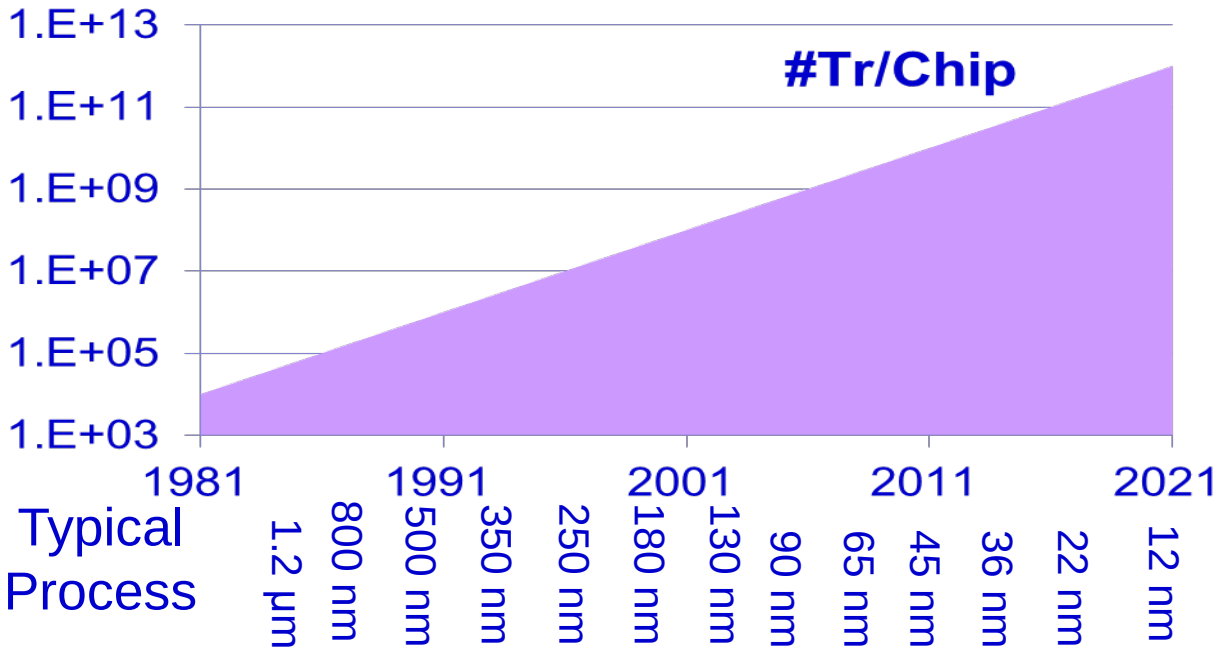
Integration of Various Technologies

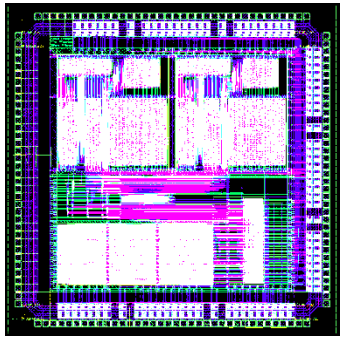
- Device Manufacture
  - Make transistors small
  - Mask Design, Exposure, Polishing, Dicing
- Circuit Design, Layout Design
  - High Speed, Low Power, Reliability
- Packaging, Printed Circuit Board
  - Wire Bonding
- System Design
- Software Design
- Marketing



Moore's law (1965)

- Gordon E. Moore (A founder of Intel)
  - #Tr/Chip doubling every 18 months (or two years)





Inevitable Paradigm Shifts

- The number of transistors in one chip becomes 100 times in every 10 years
- The smaller the feature size of VLSI chip is
  - the higher the performance of VLSI is
  - the larger the difficulty in VLSI design is

- Time-to-market constraint
- Performance (area, speed, power…) constraint

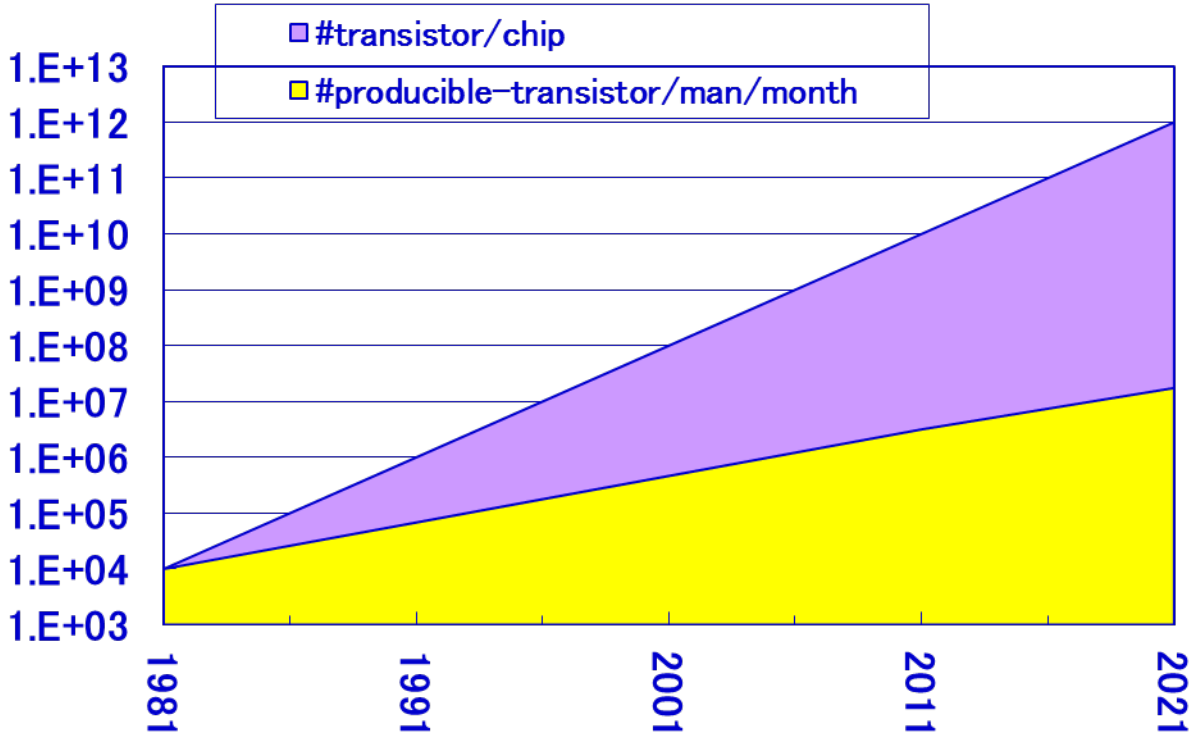
Change of Names

- IC: Integrated Circuit (1960-)
- LSI: Large Scale IC (1970-)
- VLSI: Very Large Scale IC (1980-)
- ULSI: Ultra Large Scale IC (1990-)

- System LSI
- SoC (System on Chip)
- SiP (System in Package),…

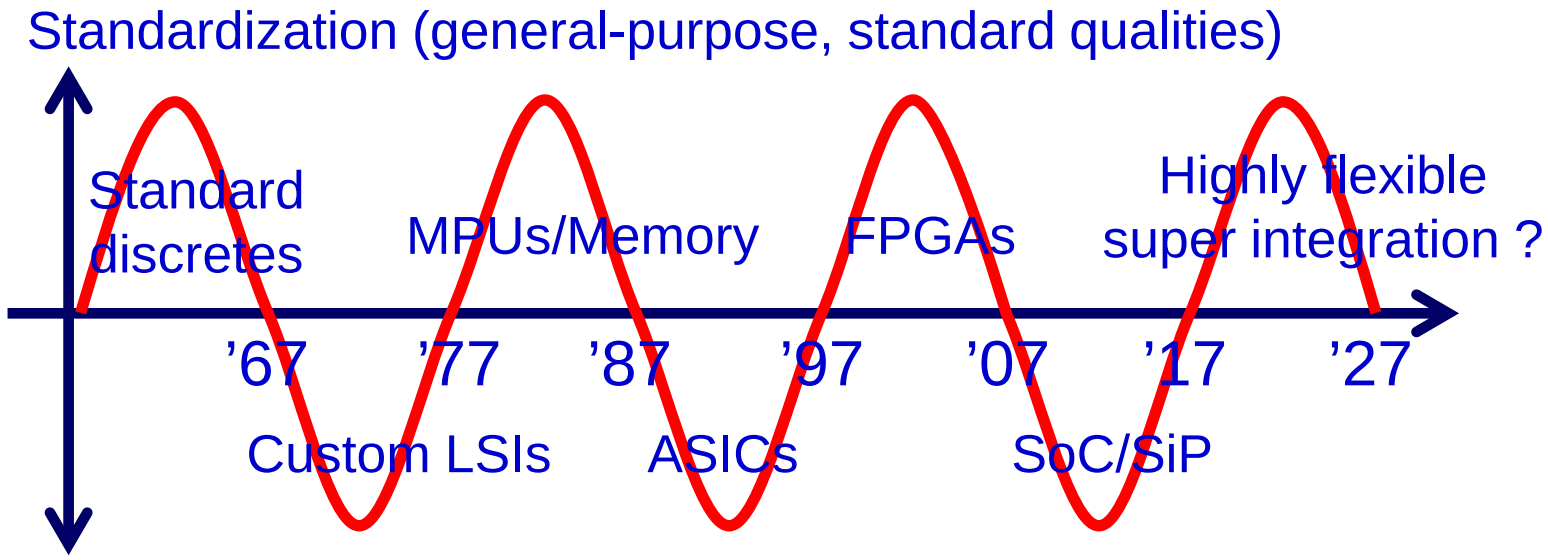
VLSI Manufacture vs. Design

- #transistor in VLSI chip +58%/year
- VLSI design productivity +21%/year



Makimoto's Wave (1987)

- Tsugio Makimoto (former Sony CTO etc.)
  - Semiconductor industry's cyclical alternation between standardization and customization



(COMPUTER, the IEEE Computer Society 2013)

Digital Integrated Circuits

- What is Digital?
  - Digital vs. Analog
    - Discrete vs. Continuous
    - Integer or Boolean (0,1) vs. Real
    - Countable vs. Uncountable
- What is Digital Integrated Circuits?
  - Realize Boolean Function: $\{0,1\}^n \rightarrow \{0,1\}^m$
  - Objective
    - Cost : Size, Speed, Power, etc.

Why Digital Integrated Circuits

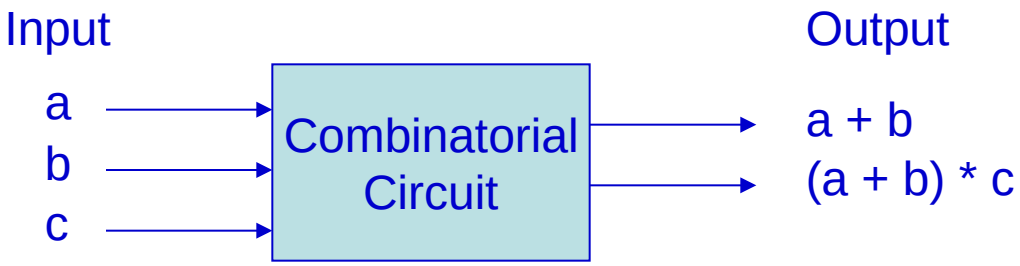
- Why Digital?
  - Digital Applications
    - Digital Signal Processing
    - Video Processing,…
  - Robustness for Instability and Uncertainty
  - High Performance and Low Cost
  - VLSI (Very Large Scale Integrated Circuit)

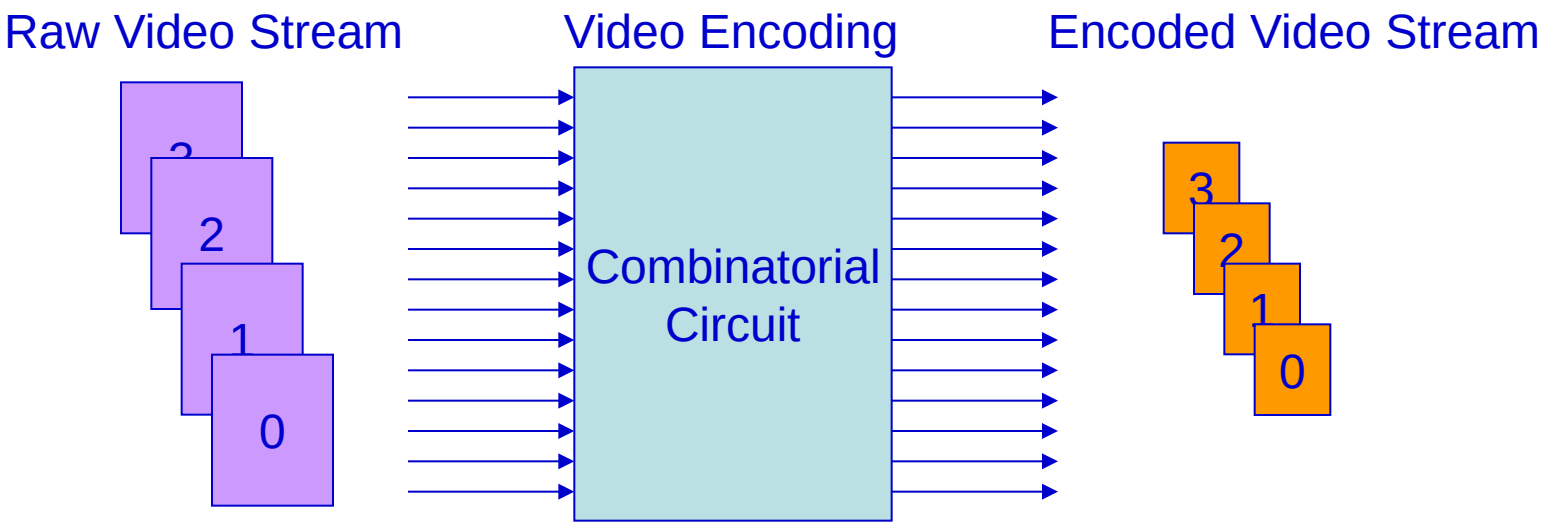
Digital System Implementation

- Combinatorial Circuits
  - Outputs are determined by Inputs
  - Every Boolean Function is realized
  - Often impractical due to size and speed
- Sequential Circuits
  - State Machine
  - Outputs are not determined only by current inputs
  - Outputs depend on input sequence as well
  - Most Digital System Implementation

Combinatorial Circuits

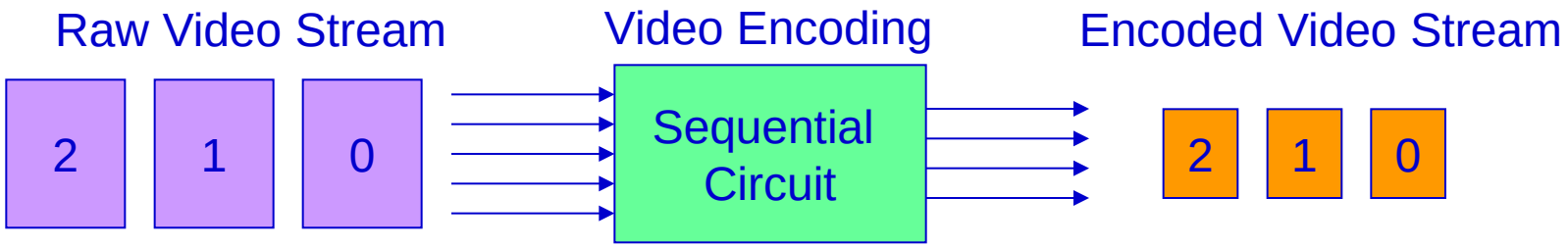
- Inputs are given at a time
- Outputs are generated at a time





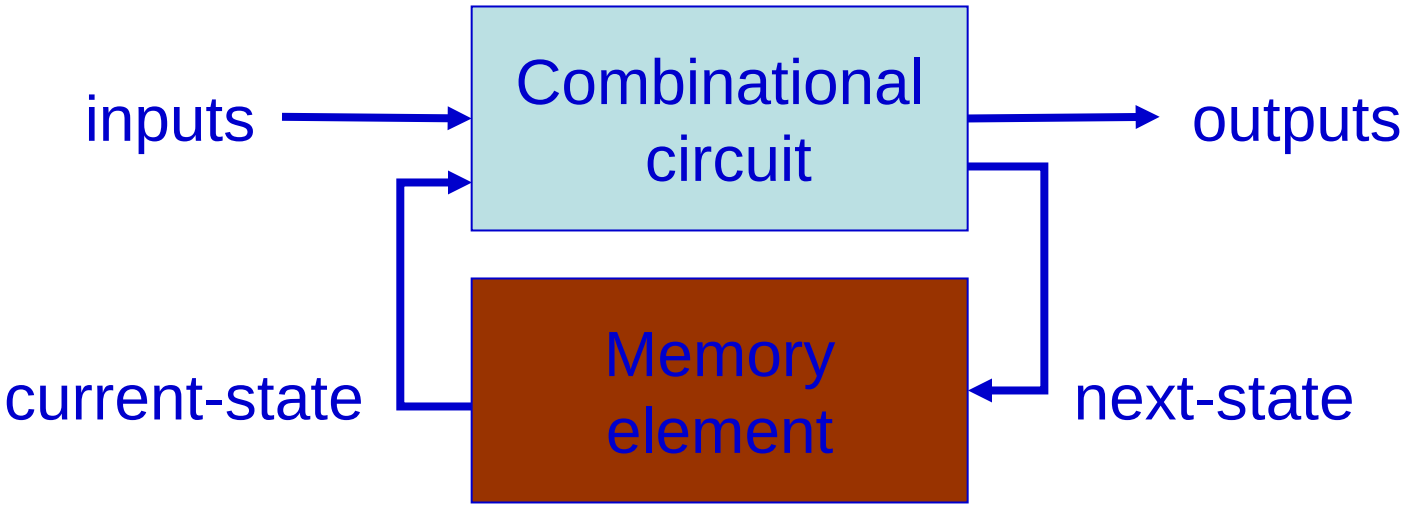
Sequential Circuits

- Inputs are given sequentially
- Input history is stored in circuit
- Outputs are generated sequentially by using inputs and stored data (history, state)



Sequential Circuit Implementation

- Performance depends on
  - State-machine itself
  - Time to transit from one state to another
    - Correct output must be recognized
    - Correct state must be stored

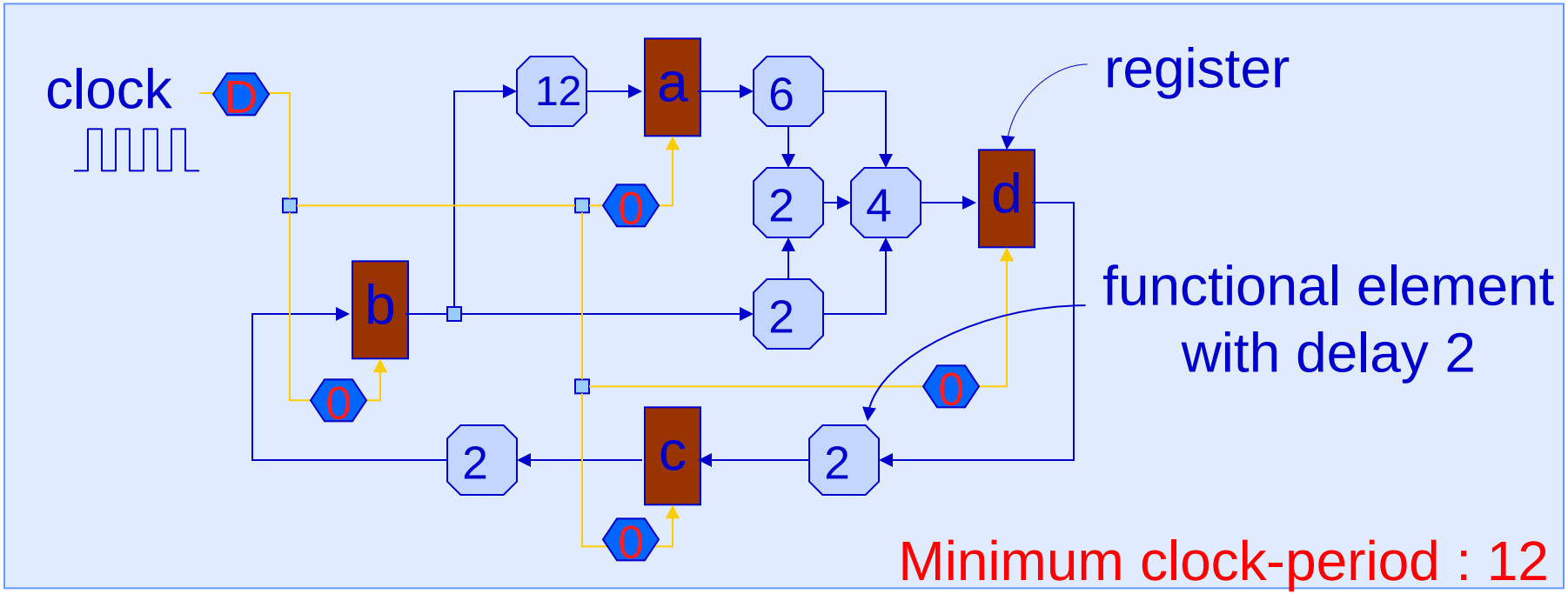


Synchronous Circuits

- Progresses in Design Automation, but still require human intelligence due to huge design space
- Synchronous Circuit Implementation
  - Synchronization by Global Clock
  - Physical Solution
- Asynchronous Circuit Implementation
  - Synchronization without Global Clock
  - Self-Synchronous
  - Logical Solution

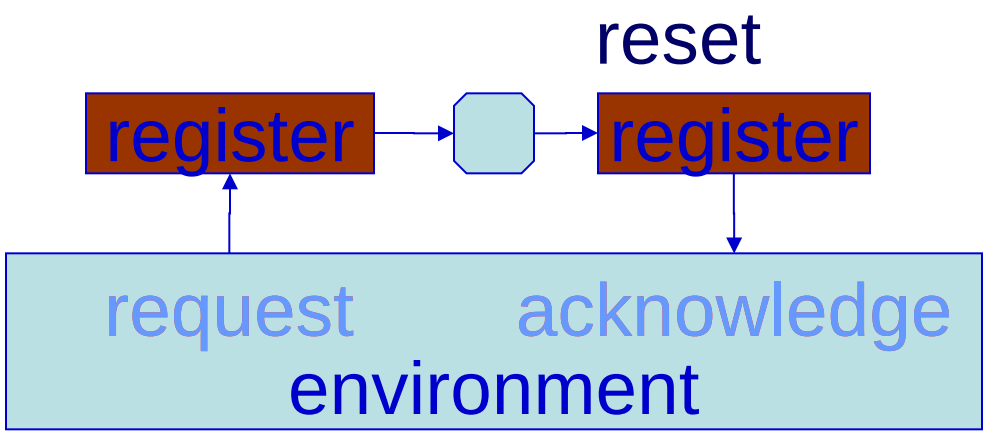
Typical Synchronous Circuits

- Every register (memory) is ticked by clock
  - Periodically (same period)
  - Simultaneously (same timing)
- Complete-synchronous circuit



Typical Asynchronous Circuits

- Synchronization by Handshake Protocol
  - Request and acknowledge
  - 2-wire 2-phase implementation



Wire value	Status
00	Not ready
01	0
10	1
11	Not valid

2-wires for 1-signal

Synchronous vs. Asynchronous

- Synchronous Circuit
  - overhead of clock circuitry
  - simultaneous clock distribution becomes harder
  - needs innovation on clock distribution
- Asynchronous Circuit
  - overhead of circuitry that guarantees stability
  - relatively slow to maintain delay insensitivity
  - needs practical delay assumption
- Mixture of Synchronous and Asynchronous Technique

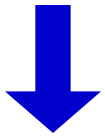
Digital Integrated Circuit Synthesis

- How to generate a Synchronous Circuit?
  - Combinatorial circuit
  - Sequential circuit

  that realizes a given Boolean Function
- Optimization Targets
  - Circuit Size
  - Speed
  - Power
  - etc.

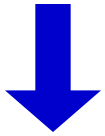
Typical VLSI Design Flow

Behavioral specification (C, VHDL, data flow graph, etc.)



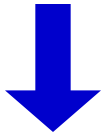
high-level synthesis

RTL description (registers, modules, MUX, etc.)



logic synthesis

Gate level circuit (NAND, NOR, etc.)

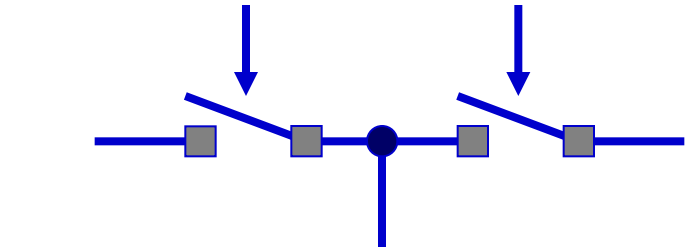


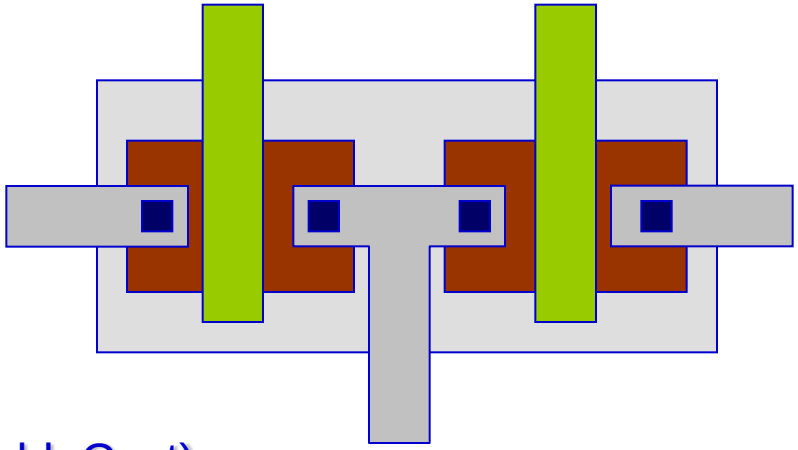
physical (layout) synthesis

Layout

Change of Design Method

- Design Method
  - Manual Design
    - Circuit Diagram, Mask
  - Computer Aided Design
    - Boring simple tasks
  - Design Automation
    - Inferior quality but used since a circuit is too big to design manually



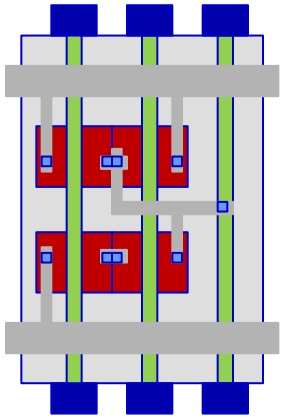


- Design Objectives
  - Area (Request from manufacturing, Yield, Cost)
  - Speed (Request from market, Emergence of PC)
  - Power (Emergence of Mobile products)
  - Noise (Influence to TV, Medical products)

Change of Design Style

History of Standardization and Abstraction

- ✓ Overcome performance degradation by scale profit
- Full Custom Design
- Semi Custom Design
- Standard Cell
  - Same cell height
- Gate Array
  - Same transistor layout
- FPGA (Field Programmable Gate Array)
  - Same logic elements
- Reconfigurable
- IP base

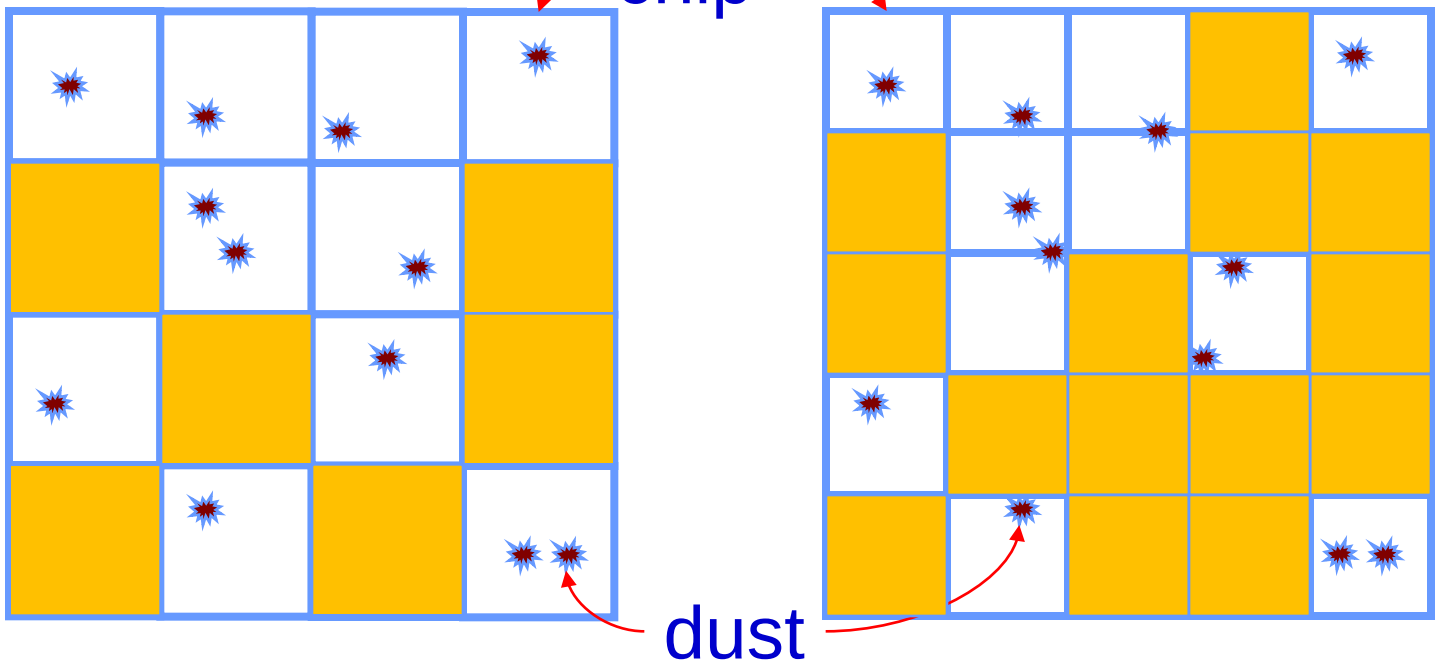


Design Objective : Chip Area Reduction

More chips and more earnings

Chip Area: Large

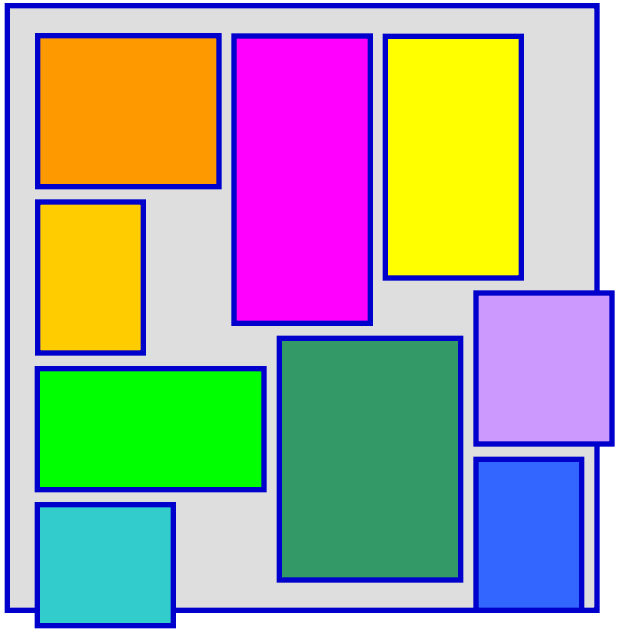
Small



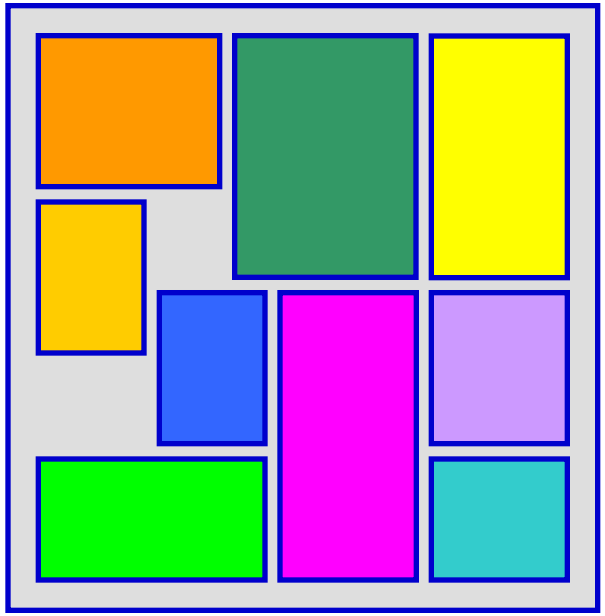
16	#chip	25
6	#actual chip	14

Packing Problem

- Not so difficult if the number of modules is small
- An optimal solution can not be found in practical time in general if the number of modules is large
- In VLSI design, routing should be taken into account



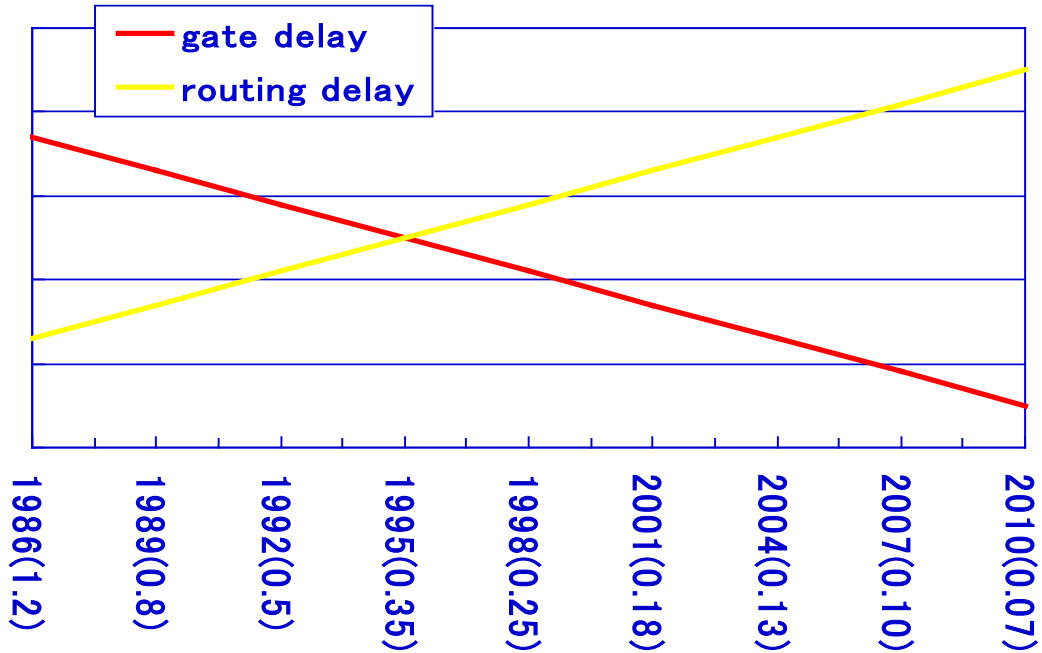
bad

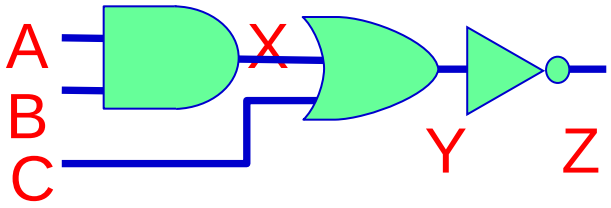


good

Design Objective : Delay Minimization

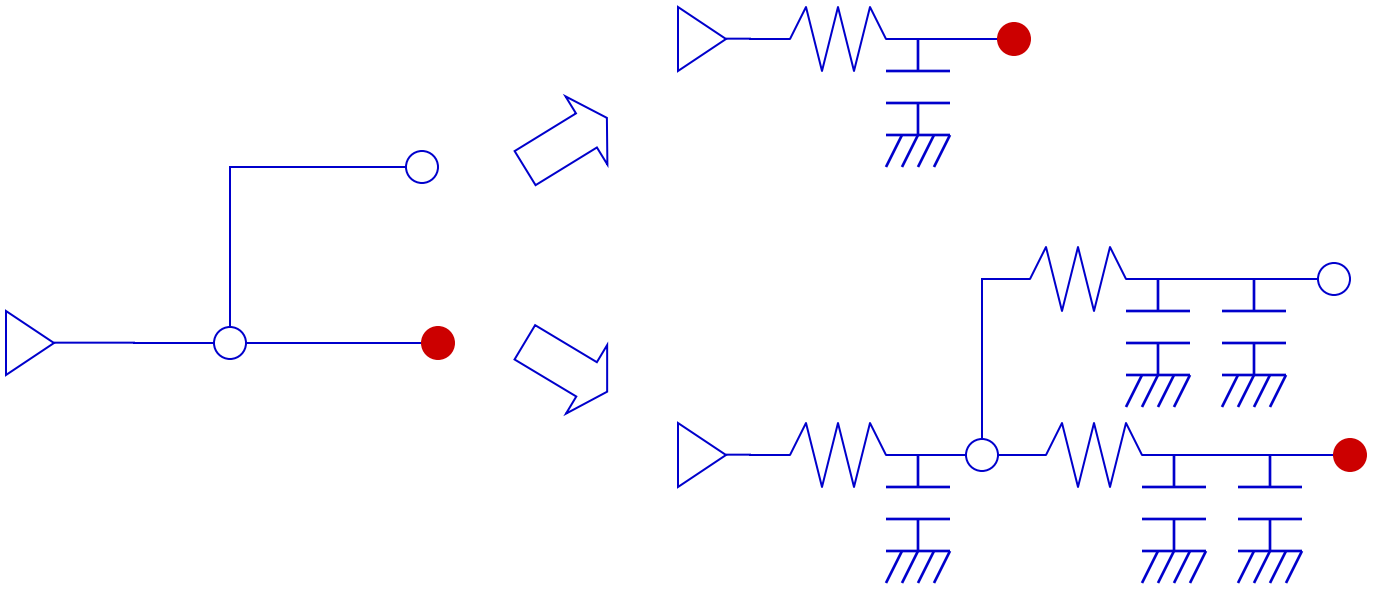
- Delay characteristics changes
  - Feature size becomes small, then
    - transistor switching speed increases
    - wire resistance increases





Delay Model Evolution

- Previous: routing delay = length
- Current: routing delay = length + distance
- Future: more accurate model is necessary

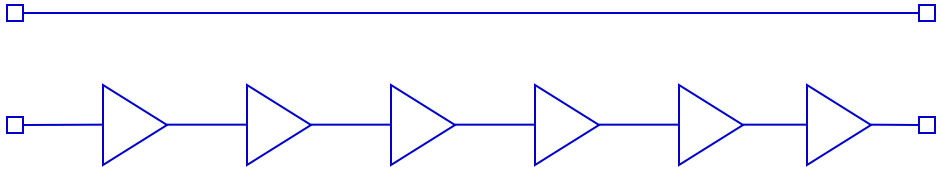


Growth of Layout Importance

- Signal Delay Estimation
  - Previous: gate level consideration is enough
    - signal delay is proportional to #gate

      routing hardly affect signal delay
  - Future: layout consideration is essential
    - signal delay depends on its path

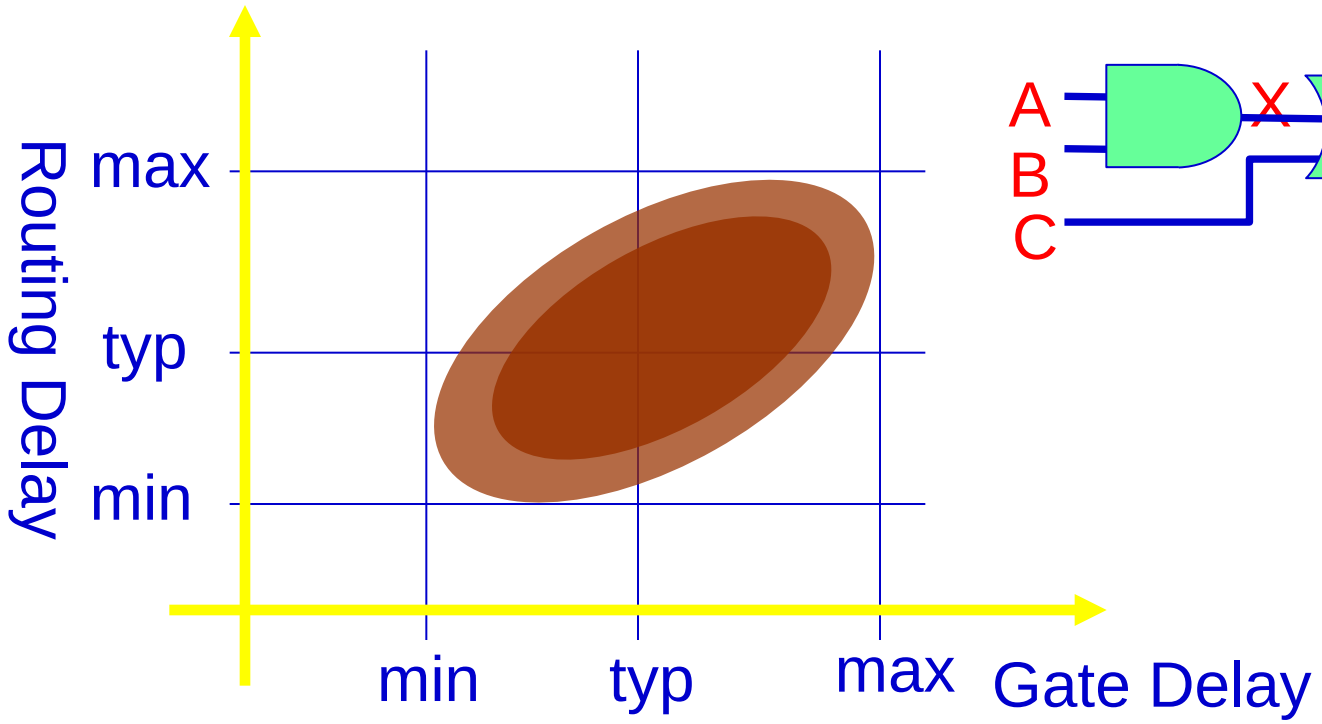
      existence of gate hardly affect signal delay



same delay?

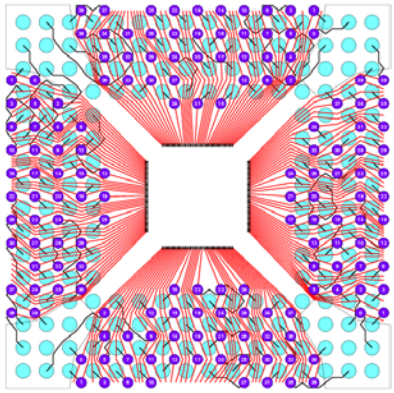
Increase in Delay Uncertainty

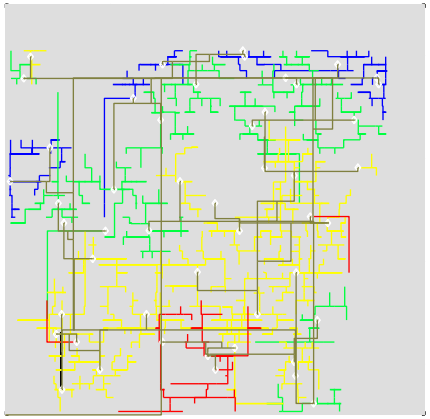
- Delay variation increases
  - System should work correctly
    under the predefined range of conditions
  - Robustness against delay uncertainty becomes important



Routing

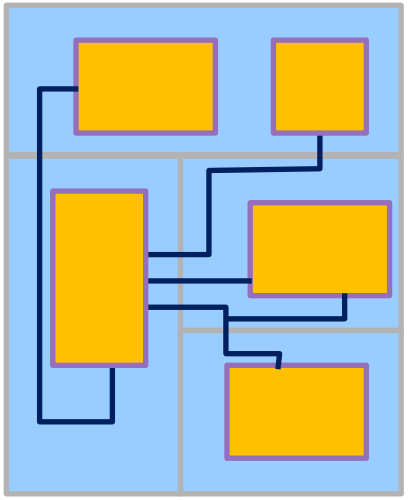
- Connect pins under the design rule
  - Many nets (many connection requests)
  - 100% completion ratio
    - 100% without manual correction
    - Near 100% + manual correction
  - Various design rules
    - # of layers
    - Obstacles
  - Various properties of instances
    - Pin distribution
  - Various objectives
    - Total length, delay, power, shape



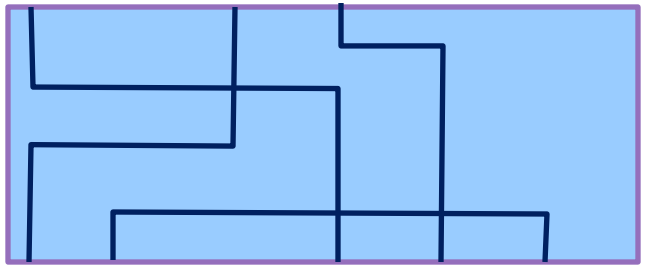


Hierarchical Design

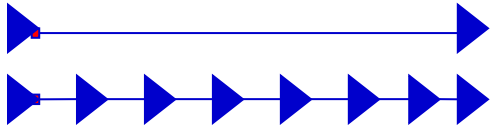
- Global routing
  - Design rule insensitive
  - Routing area is divided into subareas
  - Balance the congestion of subareas
    - Greedy approach
      - Shortest Path (Two terminal)
      - Steiner Tree (Three or more terminal)
    - Rip-up and Reroute

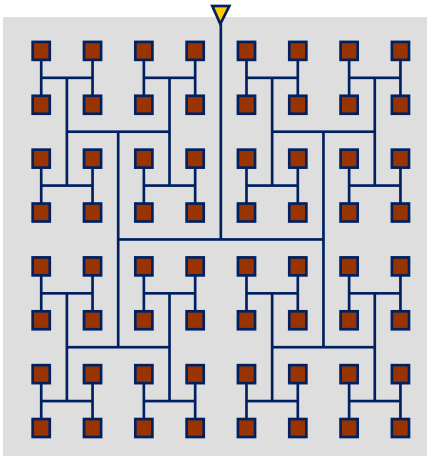


Hierarchical Design



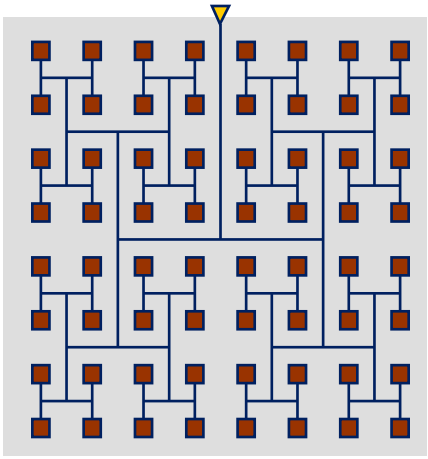
- Detailed routing
  - Design rule sensitive
  - Multiple Nets
    - Channel routing (Two or Three layer)
    - Switch box routing (Two or Three layer)
    - Area routing (Three or more layer)
  - Single Nets
    - Wire sizing
    - Buffer Insertion
    - Signal integrity
    - Via planning
    - Clock routing

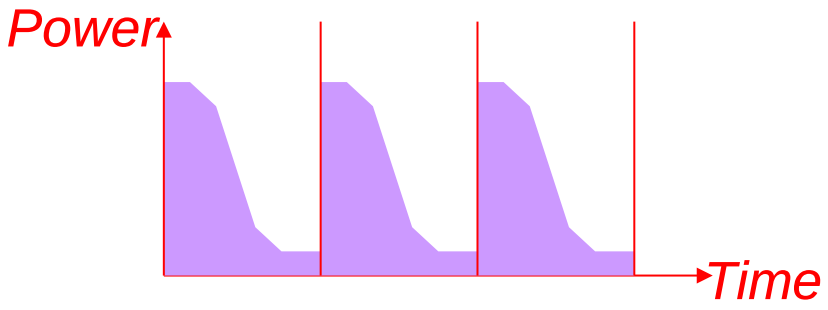




Objectives

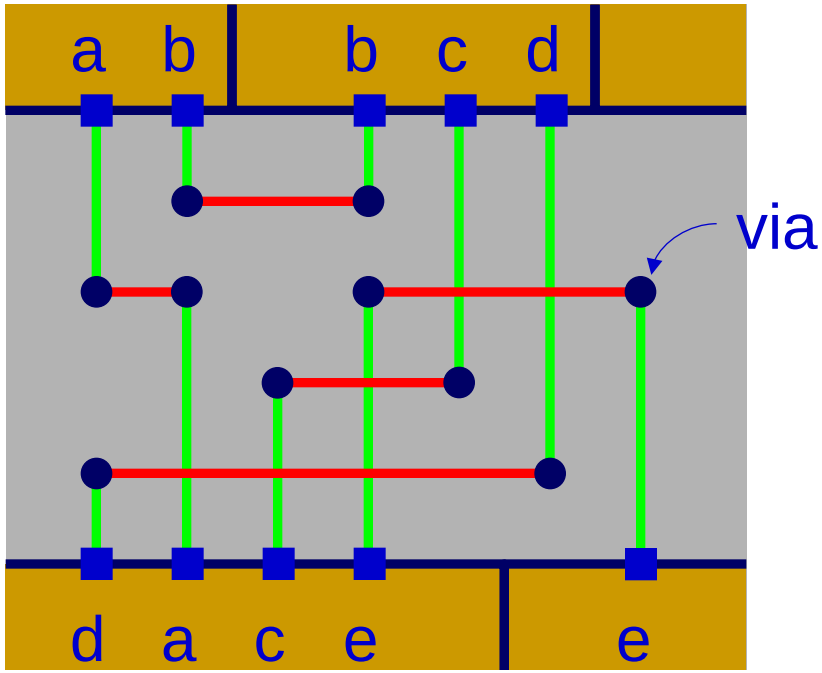
- Objectives are changing depending on technological environments
  - 100% routing
  - Area (total length) minimization
  - Delay minimization
  - Skew minimization
  - Power minimization
  - Noise minimization
  - Delay control



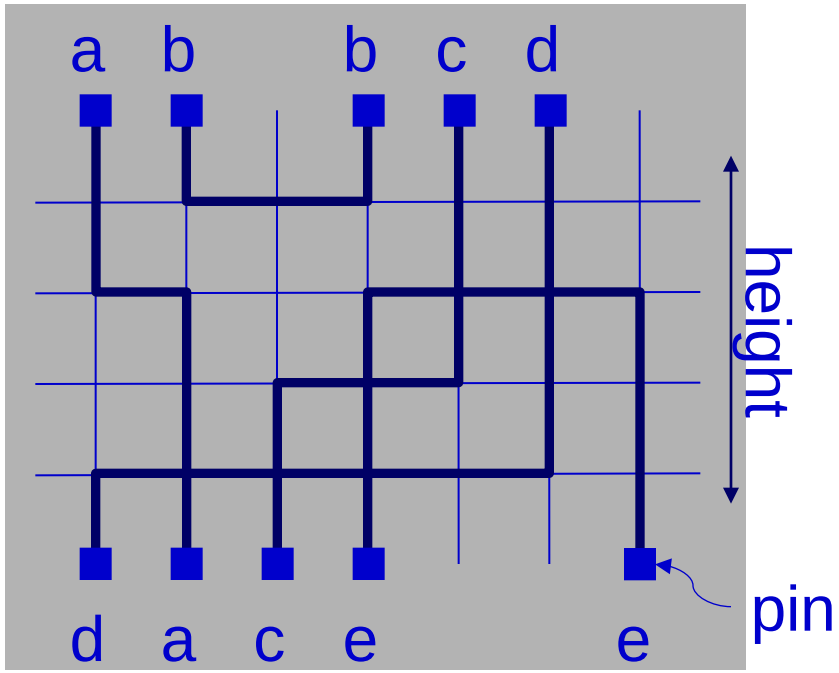


Design Objectives in Channel Routing

- 2-Layer Channel Routing
  - Connect pins on the boundary of routing area using 2-layer
  - Minimize the number of tracks (height, width) of channel



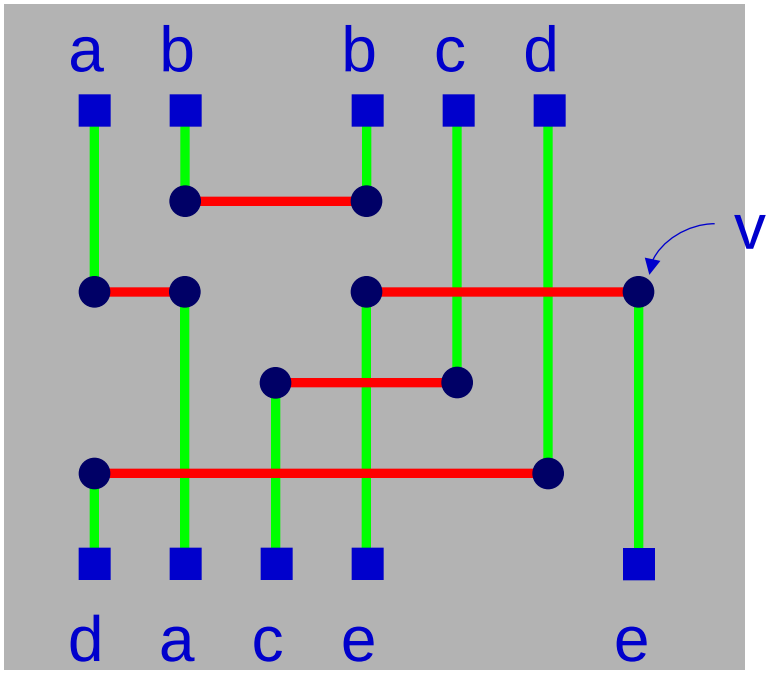
HV rule



Via Problem

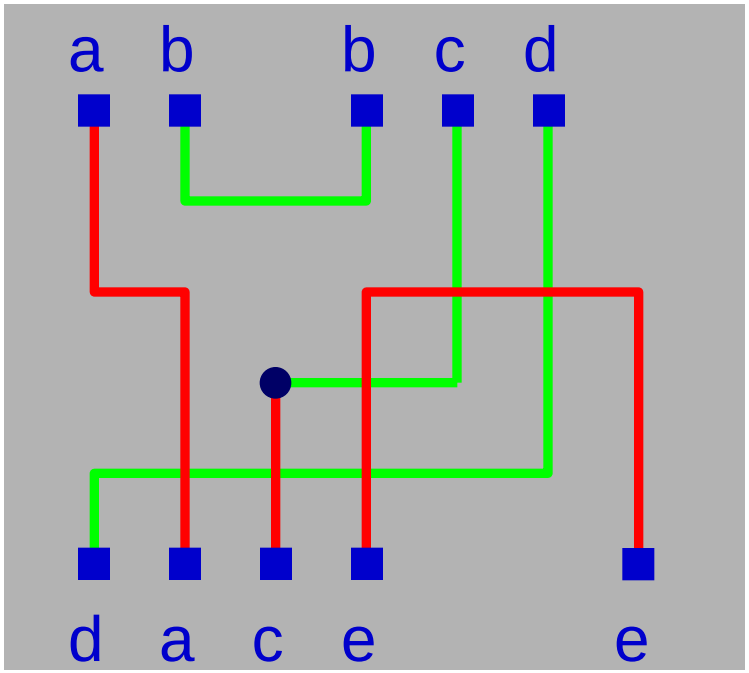
- Via Minimization
  - Minimize #via by assigning wires into proper layer

#via = 10



HV rule

#via = 1

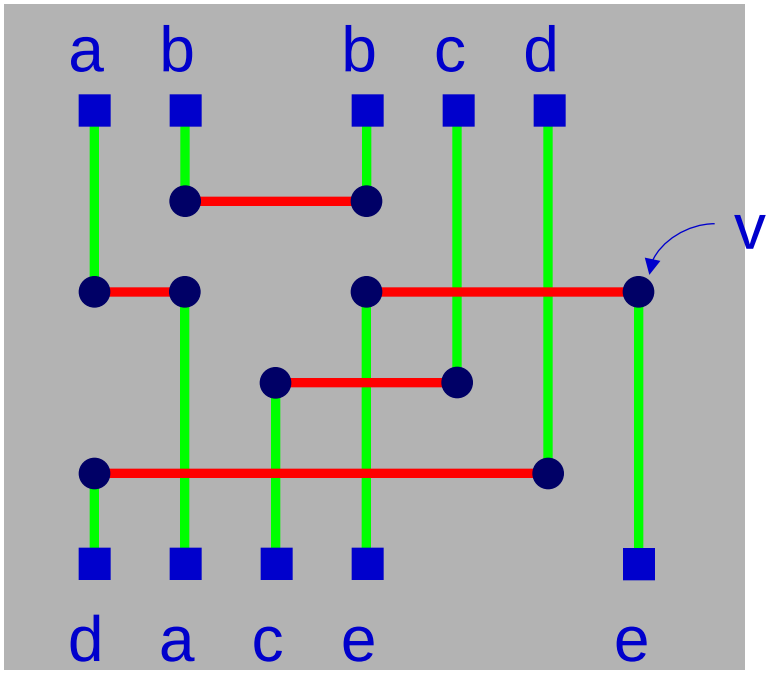


arbitrary rule

Via Problem (2)

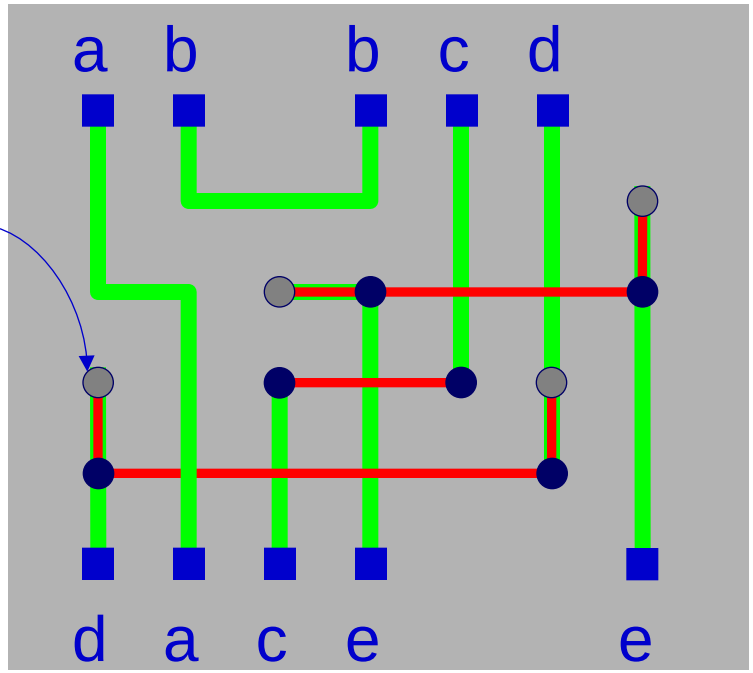
- Double Via Insertion
  - Minimize #single-via to improve the reliability

#single-via = 10



via

#single-via = 2



Boolean Function

- Boolean Function f : $B^n \rightarrow B^m$
  - Input variables : $x_1, x_2, \ldots, x_n$ (in B)
  - Output variables : $f_1, f_2, \ldots, f_m$ (in B)

- Boolean Set B
  - { 0, 1 }
  - { False, True }
  - { GND, VDD }
  - is represented by the voltage of a node in a circuit
    - 1 : high voltage (say 5[v])
    - 0 : low voltage (say 0[v]
- Boolean variable : takes values in B

Example: Summation

- Number Notation
  - Integer (Unsigned)

dec.	binary	hex
0	0	0
1	1	1
2	10	2
3	11	3
4	100	4
5	101	5
6	110	6
7	111	7
8	1000	8

dec.	bin.	Hex
9	1001	9
10	1010	A
11	1011	B
12	1100	C
13	1101	D
14	1110	E
15	1111	F
16	10000	10
17	10001	11

  - Signed Integer
    - 2's-complement

dec.	binary
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111

dec.	binary
-8	1000
-7	1001
-6	1010
-5	1011
-4	1100
-3	1101
-2	1110
-1	1111

Enable efficient circuit synthesis

Example: Summation

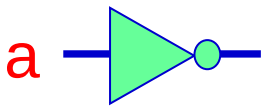
- X+Y
  - + : B^2 x B^2 → B^3
  - + : B^4 → B^3
- Input
  - two 2-bit binaries
    - X: (x_1, x_0)
    - Y: (y_1, y_0)
- Output
  - one 3-bit binary
    - X+Y : (f_2 ,f_1, f_0)

X	Y	X+Y
0	0	0
0	1	1
0	10	10
0	11	11
1	0	1
1	1	10
1	10	11
1	11	100

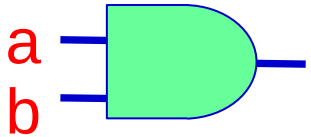
X	Y	X+Y
10	0	10
10	1	11
10	10	100
10	11	101
11	0	11
11	1	100
11	10	101
11	11	110

Basic Logic Gates

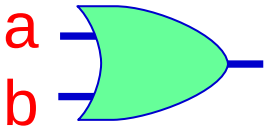
- NOT gate (Inverter)
  - Output = ¬Input
- AND gate
  - Output = Input1^ Input2
  - Looks like production (times)
    - often write as Y=AB
- OR gate
  - Output = Input1 v Input2
  - Looks like summation (plus)
    - often write as Y=A+B



¬ a | $\overline{a}$ | a’



a ^ b | ab



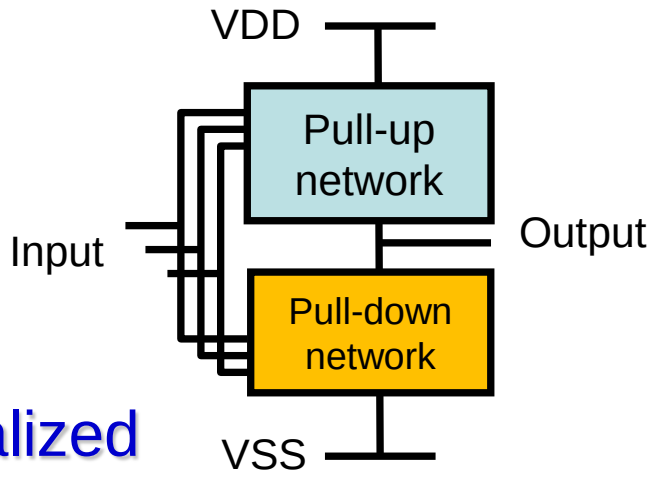
a v b | a + b

Logic Synthesis

- Get a small logic circuit that realizes a given Boolean function
  - NP-hard problem
  - Exact methods
    - Exponential time algorithm
  - Heuristics
    - Good quality
- Smallest logic circuit is not necessarily optimum
  - Objectives are Size, Delay, Power and etc.

CMOS Implementation

- Complementary Metal-Oxide-Silicon
- Pull-up and pull-down transistor networks
  - Larger area
  - Low power

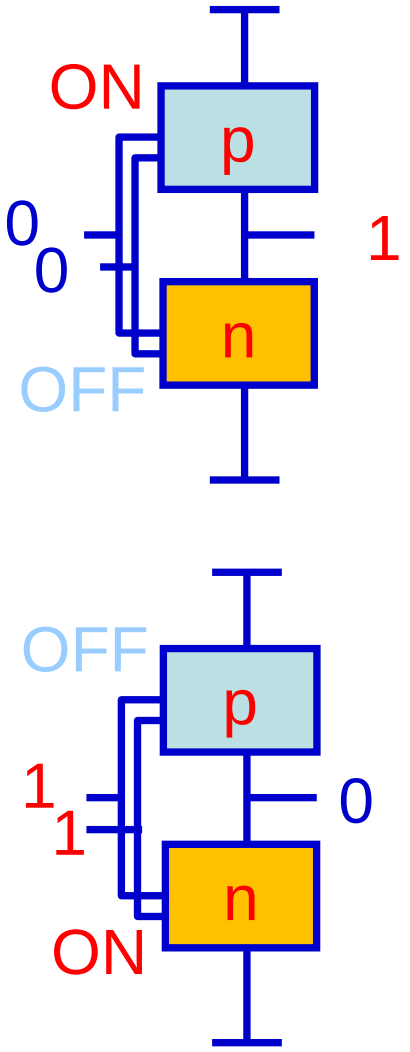


- Single-stage CMOS
  - Complex function can be realized
    - May cause area and/or speed overhead
    - AND / OR functions can not be realized

CMOS Property (1)

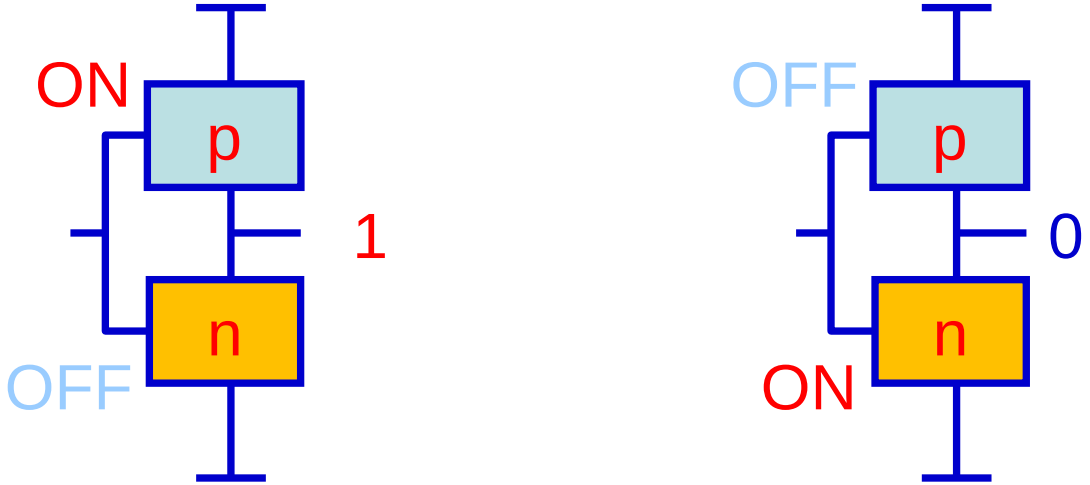
- When all inputs are 0
  - Pull-up is ON
  - Pull-down is OFF
  - Output is 1
- When all inputs are 1
  - Pull-up is OFF
  - Pull-down is ON
  - Output is 0

Cannot realize AND, OR functions



CMOS Property (2)

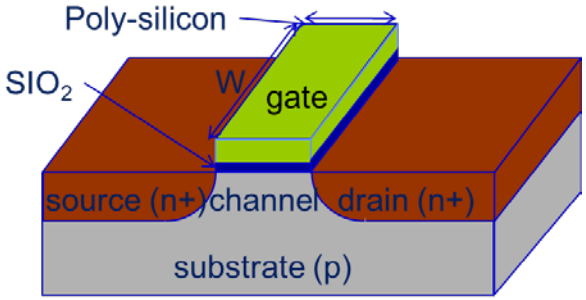
- Pull-up and pull-down transistor networks operate complementary
  - When Pull-up is ON, Pull-down is OFF
  - When Pull-up is OFF, Pull-down is ON

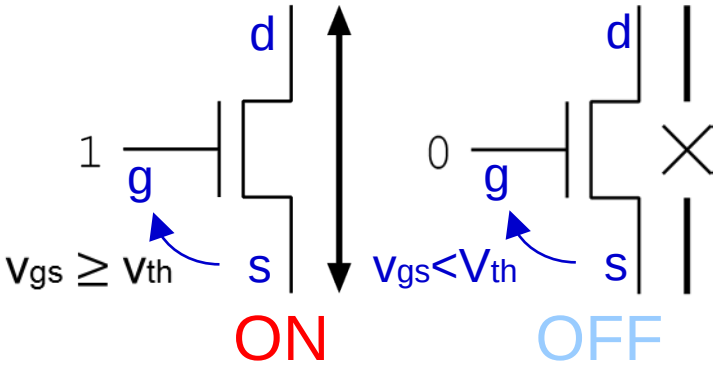


Low Power since no direct current from VDD to VSS

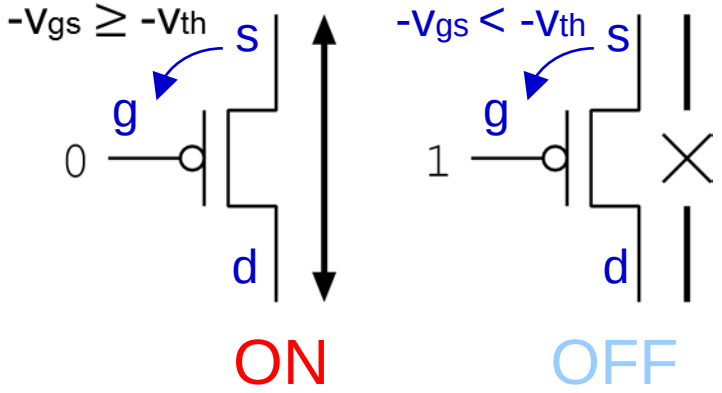
nMOS and pMOS Transistors

- nMOS (npn)
  - ON when gate is high
  - OFF when gate is low

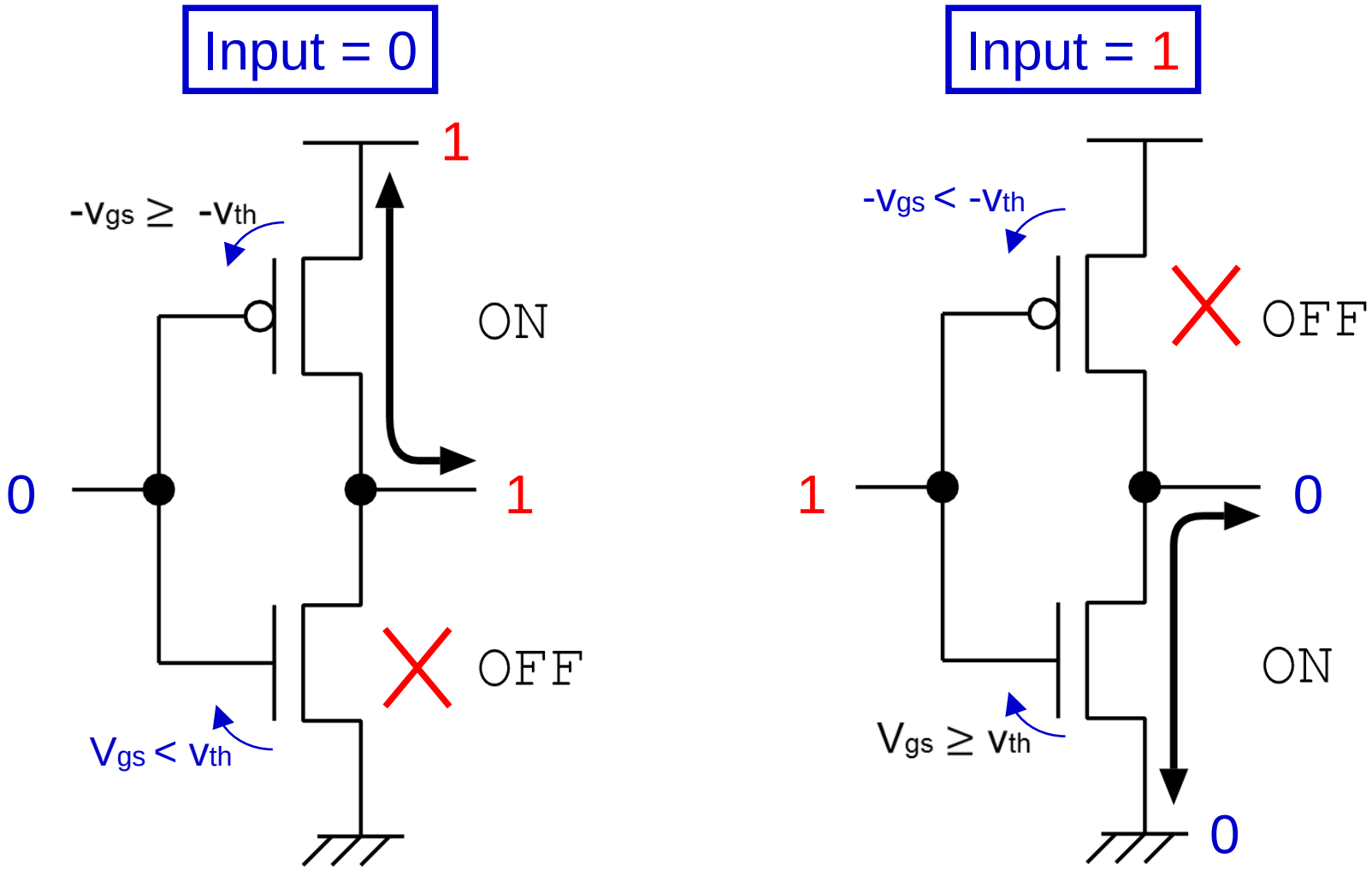




- pMOS (pnp)
  - ON when gate is low
  - OFF when gate is high

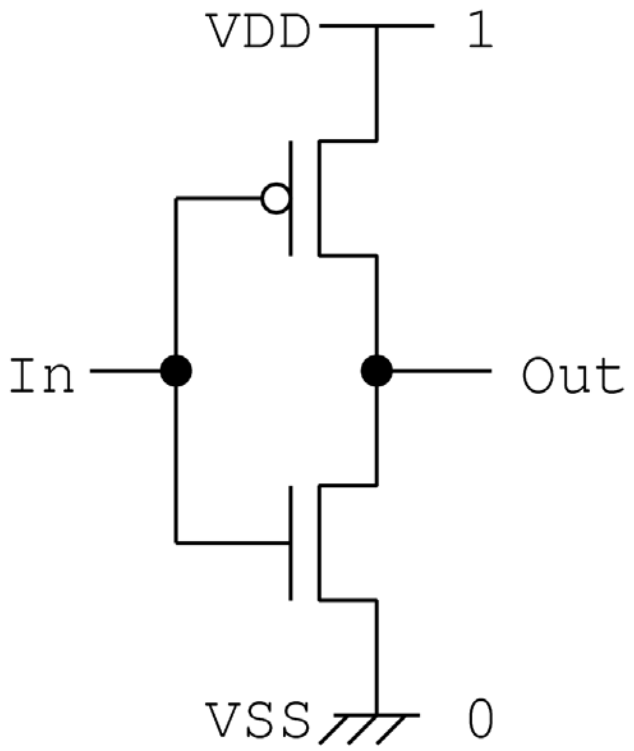


CMOS NOT Gate Behavior

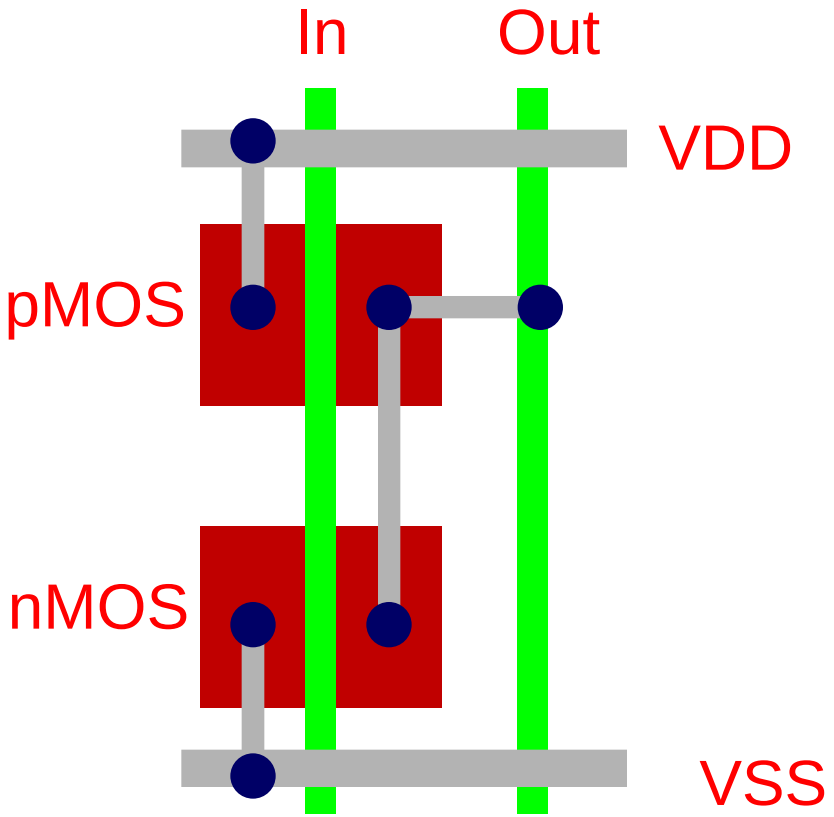


CMOS NOT Gate Layout

Circuit Diagram

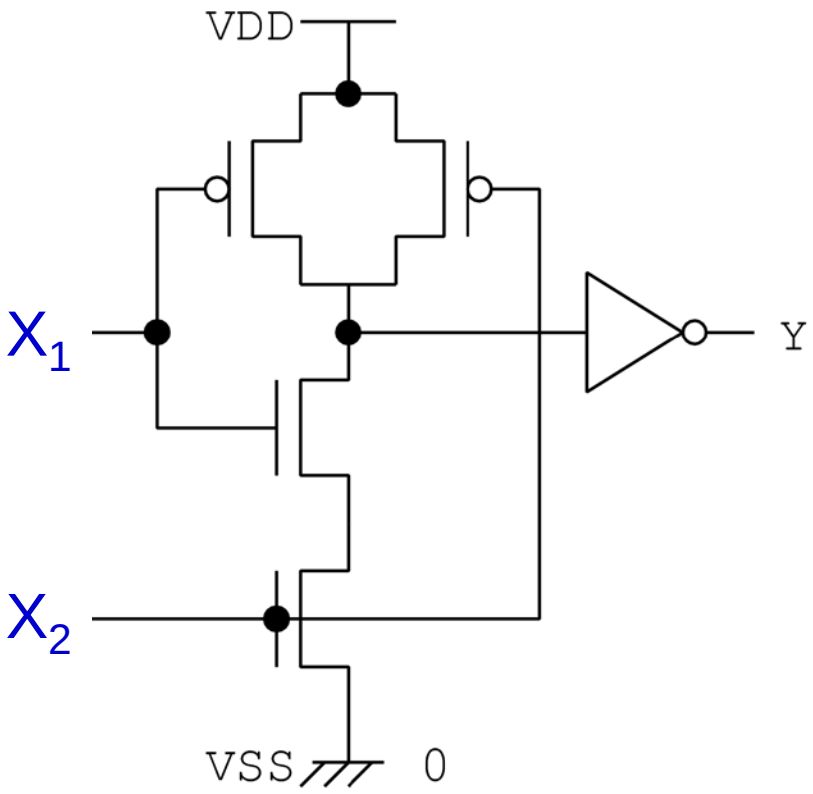


Layout Image (top view)

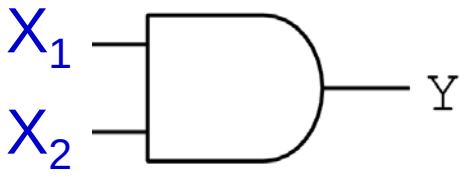


CMOS AND Gate ($Y=X_1 \wedge X_2$)

Circuit Diagram



Symbol

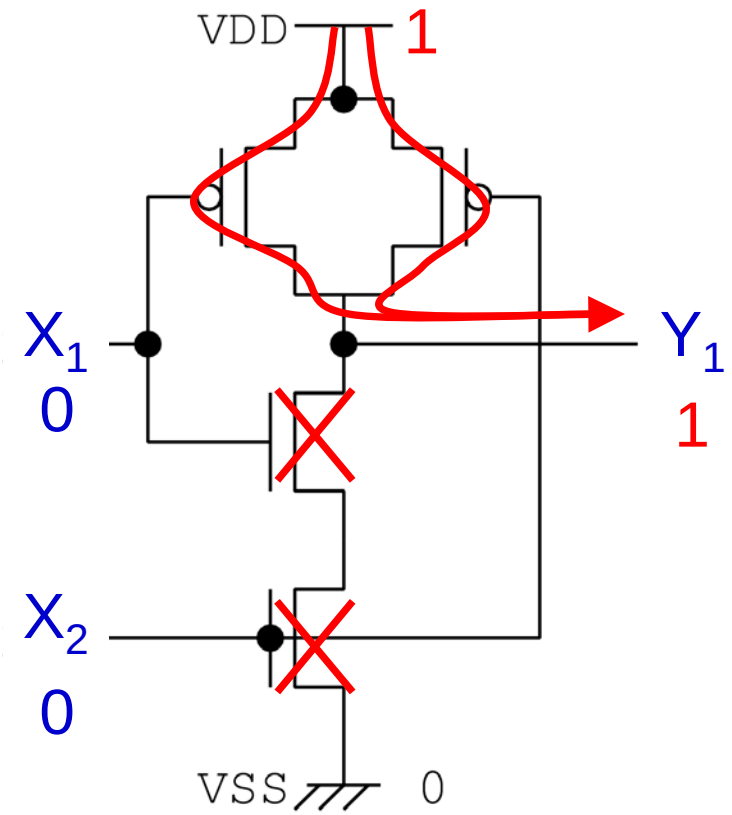


Truth Table

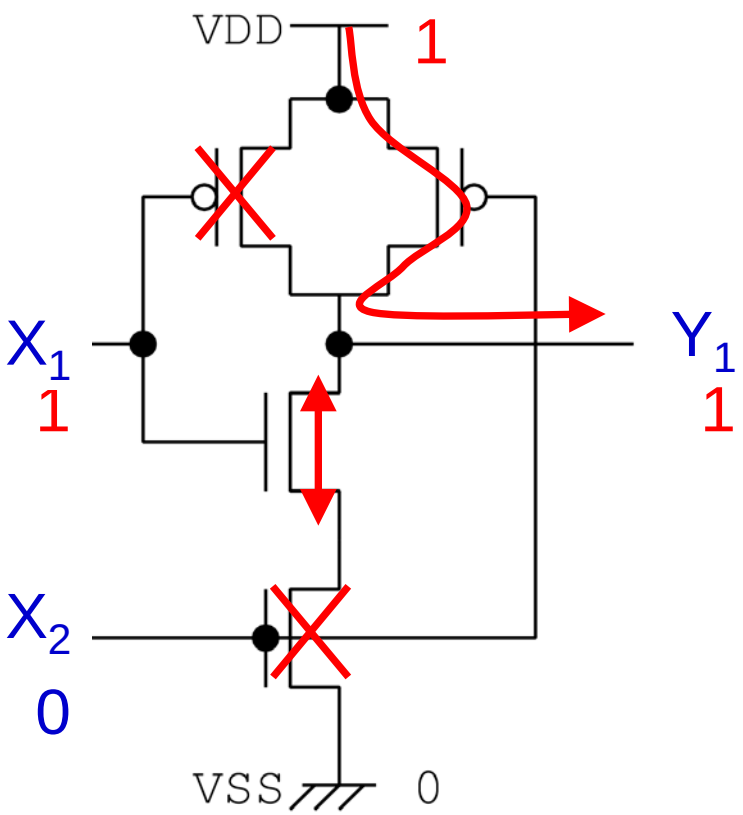
X_1	X_2	Y
0	0	0
0	1	0
1	0	0
1	1	1

AND Gate Behavior

$X_1 = X_2 = 0$

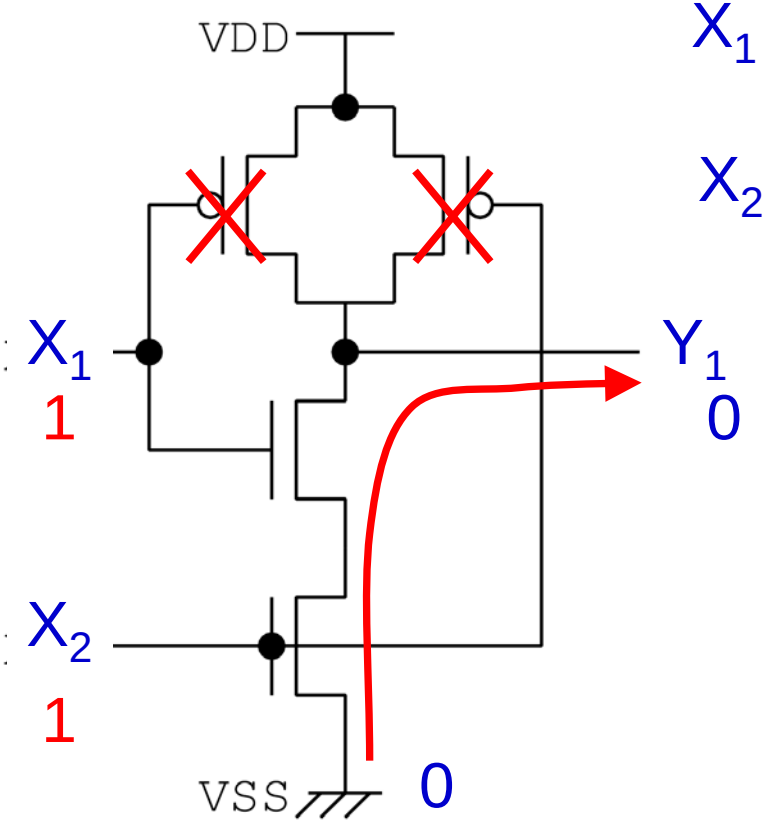


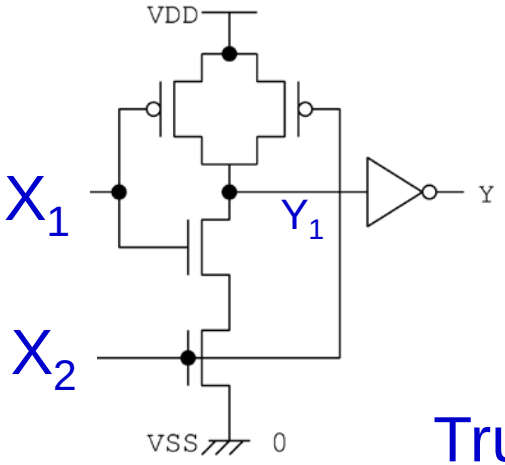
$X_1 = 1, X_2 = 0$



AND Gate Behavior (2)

$X_1 = X_2 = 1$





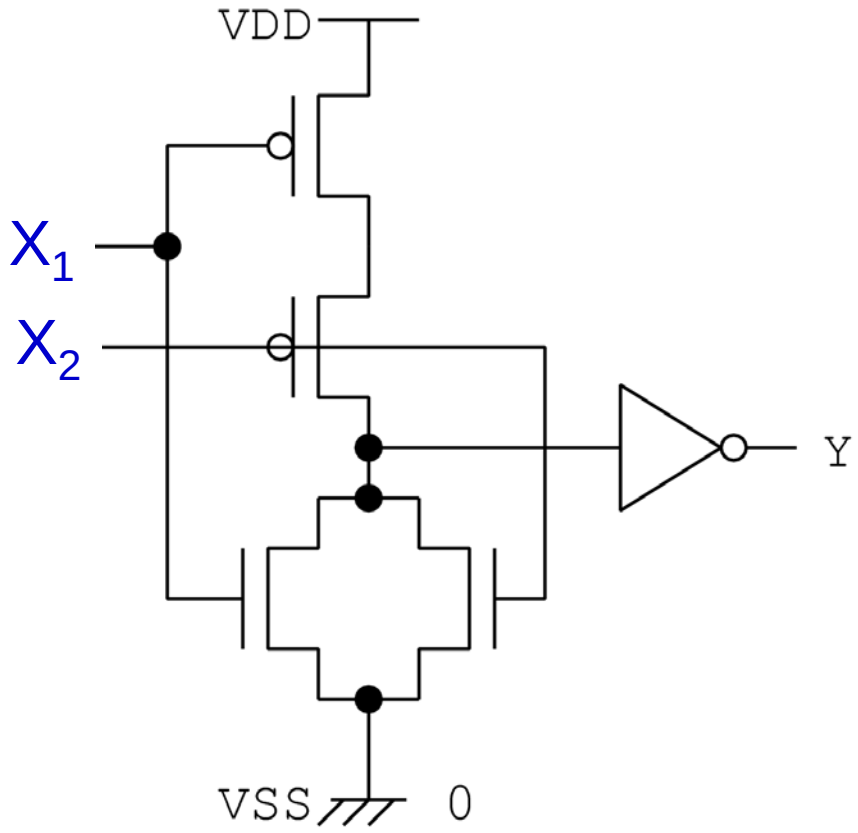
$Y = \overline{Y_1}$

Truth Table

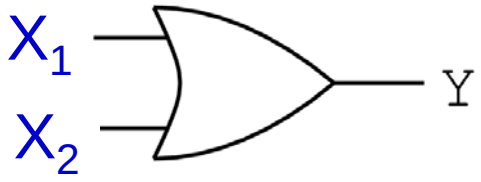
X_1	X_2	Y_1	Y
0	0	1	0
0	1	1	0
1	0	1	0
1	1	0	1

CMOS OR Gate ($Y=X_1 v X_2$)

Circuit Diagram



Symbol

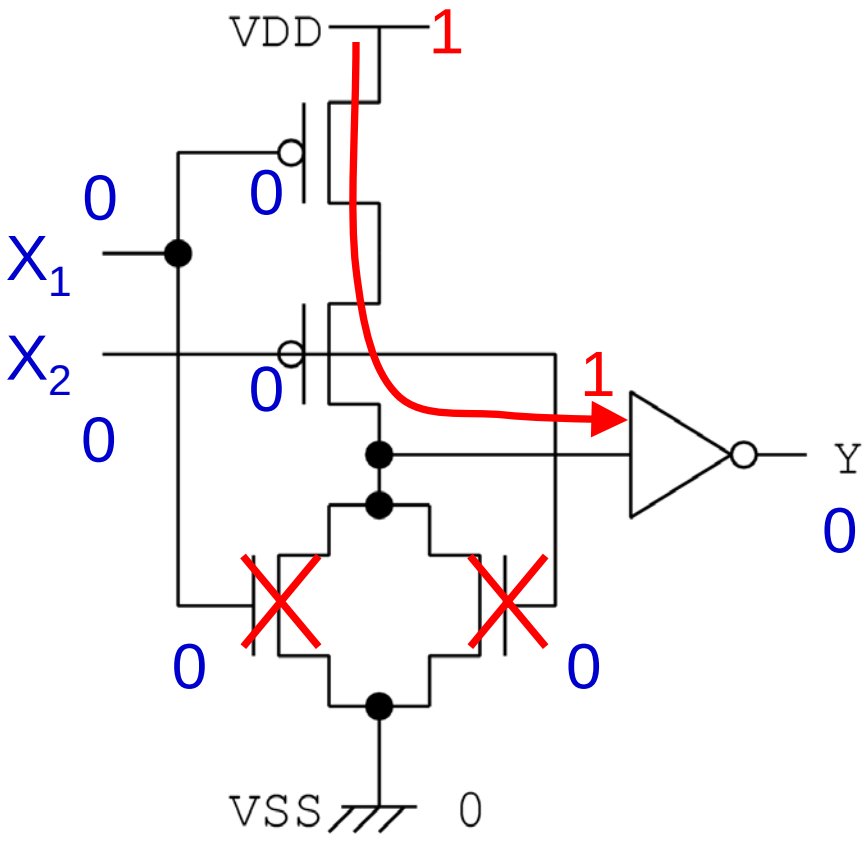


Truth Table

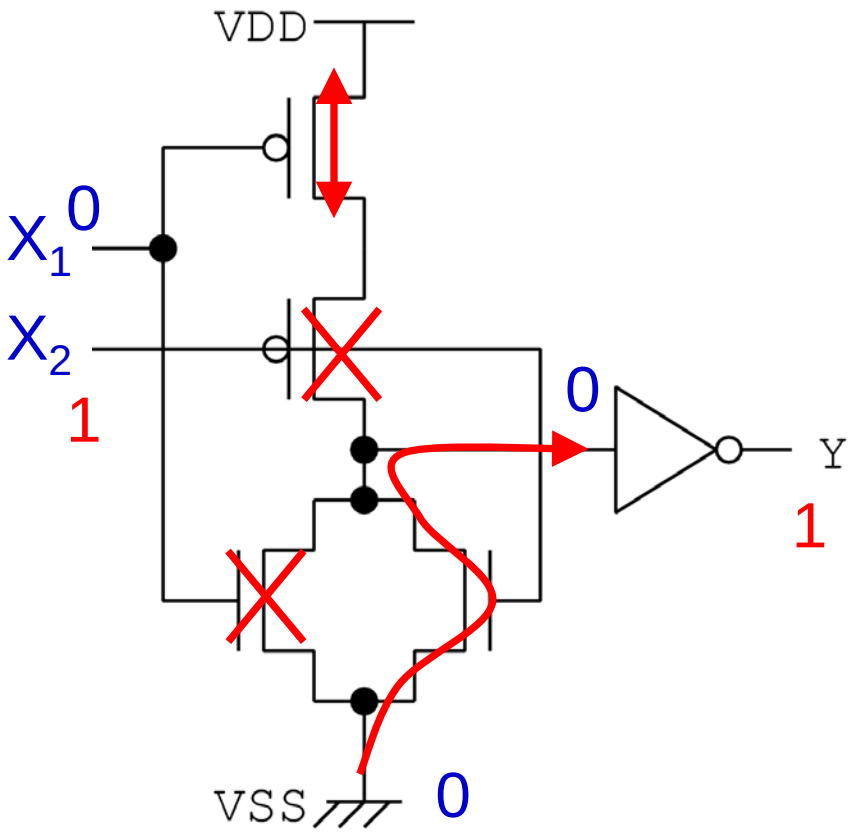
X_1	X_2	Y
0	0	0
0	1	1
1	0	1
1	1	1

OR Gate Behavior

$X_1 = X_2 = 0$

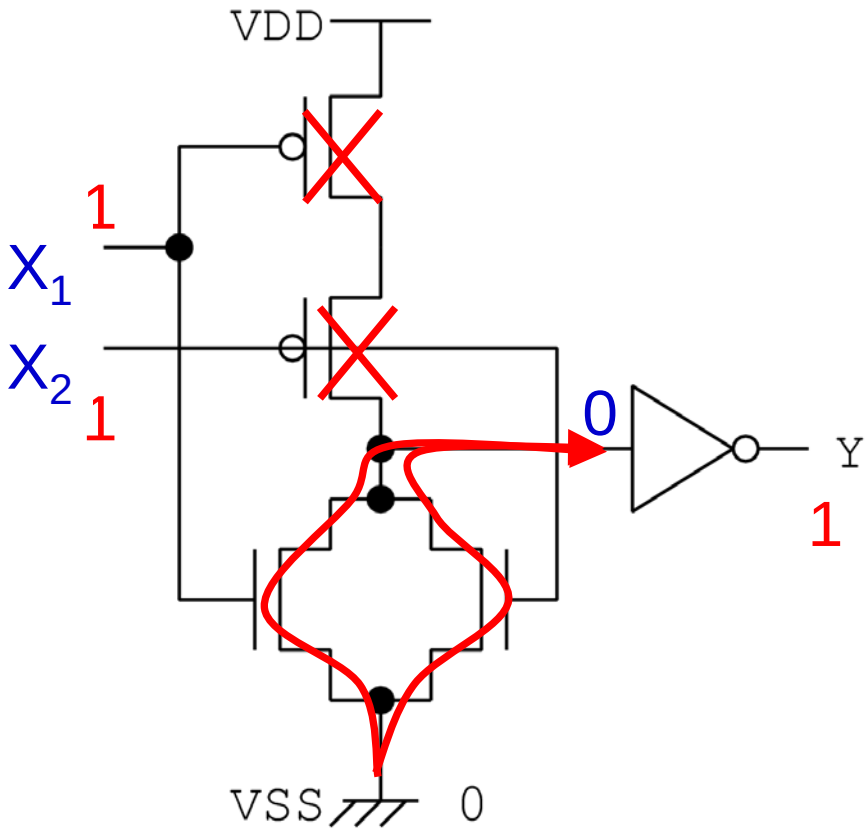


$X_1 = 0, X_2 = 1$



OR Gate Behavior (2)

$X_1 = X_2 = 1$



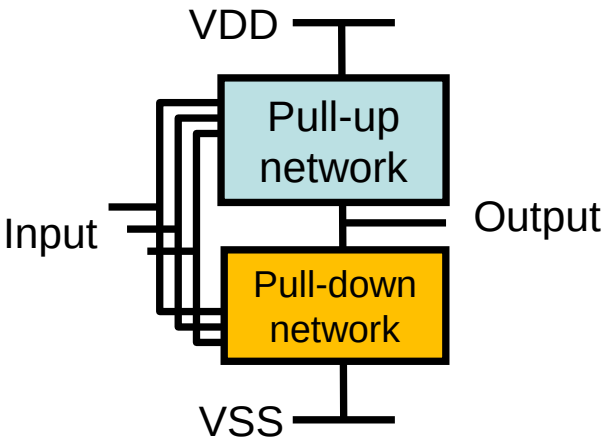
Truth Table

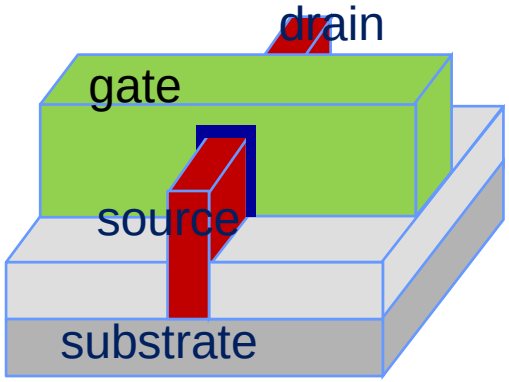
X_1	X_2	Y_1	Y
0	0	1	0
0	1	0	1
1	0	0	1
1	1	0	1

$Y = \overline{Y_1}$

CMOS Challenges

- Lower supply voltage
  - Increase of leak current
  - Dynamic power vs. Static power
- New Devices
  - FinFET
    - gate wraps around the channel or “fin”
  - 3D Integration
  - ✓ Different properties





VLSI and Computer System

- Integration of Various Technologies
- Roadmap
  - Need technologies on an appropriate timing
    - One missing technology ruins whole
    - Technology too early to use might be wasteful