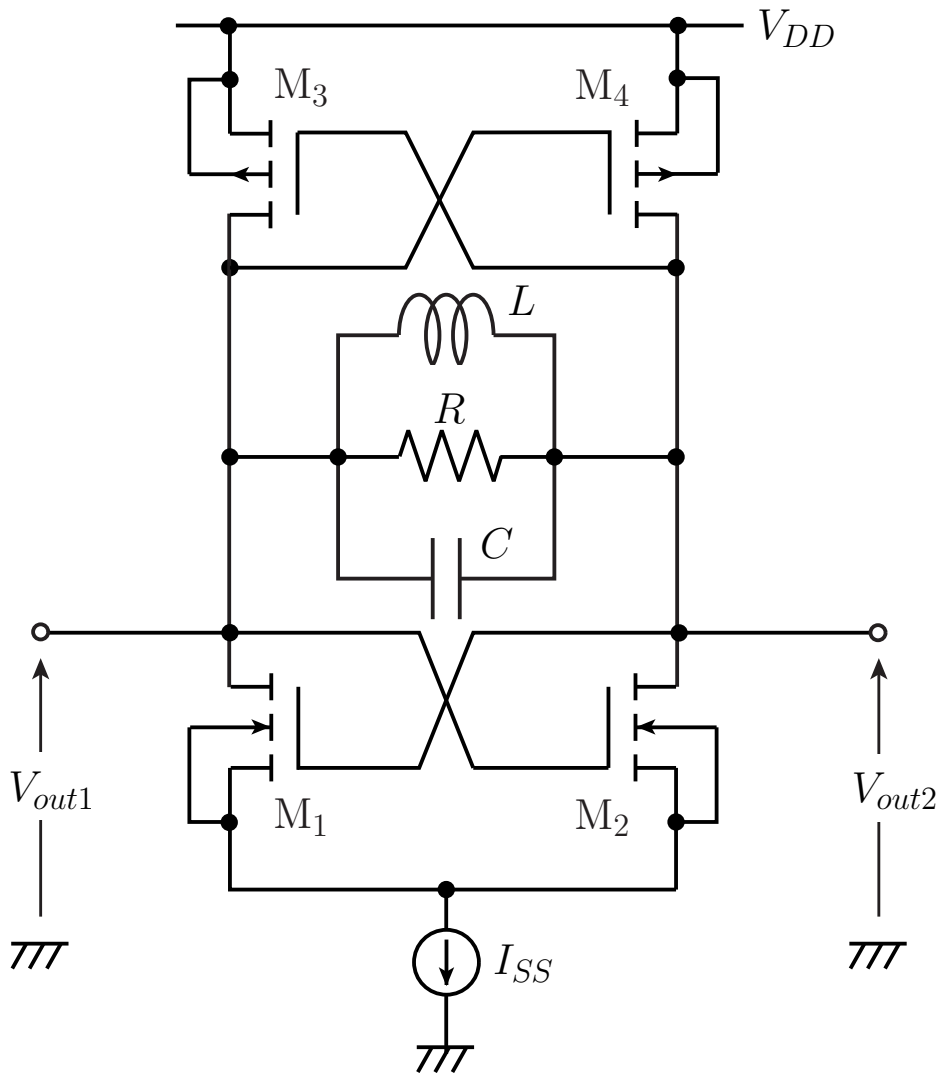
Low-Power and Area-Efficient Active Inductor Realizations

Challenge: GHz-Band Analog Circuit Design

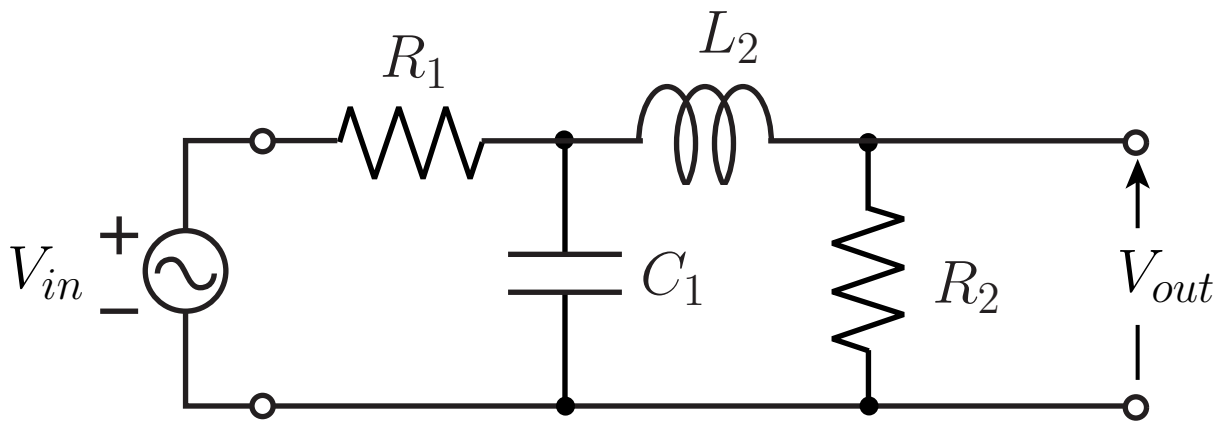
Possible Solution: Use of Inductors

- Oscillators
- Filters
- Amplifiers
- etc



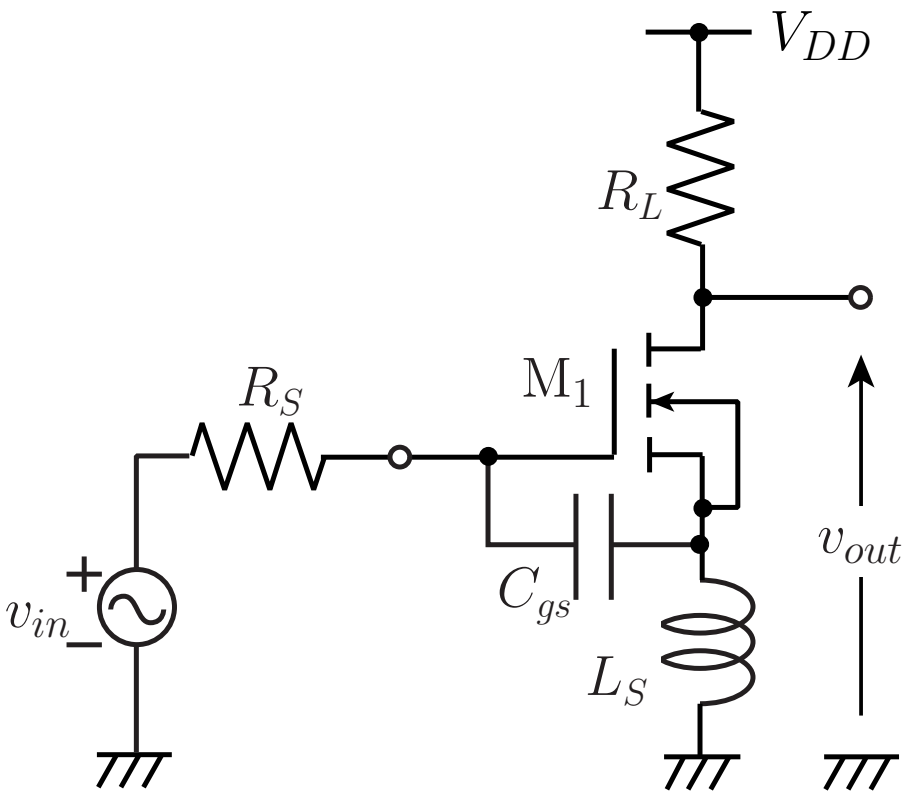
LC-tank oscillator

Low Phase Noise



2nd-order doubly terminated LC filter

Low Sensitive to Reactance Element Value Deviations



Low-noise amplifier

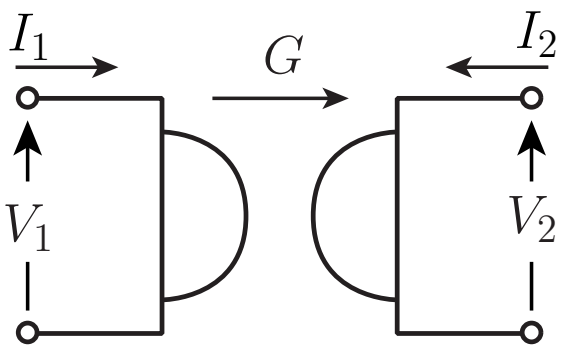
Power Matching & Low Noise

Problems

- Large Chip Area
- Poor quality (low quality factor)

Our Approach:
Novel Active Inductor Implementation

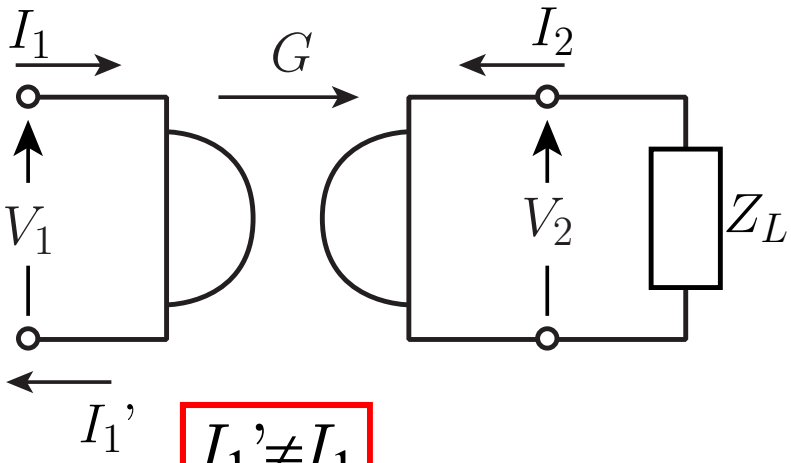
Conventional Approach: Use of Gyrators



Symbol of gyrator

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} 0 & \pm G \\ \mp G & 0 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$$

Y matrix for gyrator



$$\boxed{I_1' \neq I_1}$$

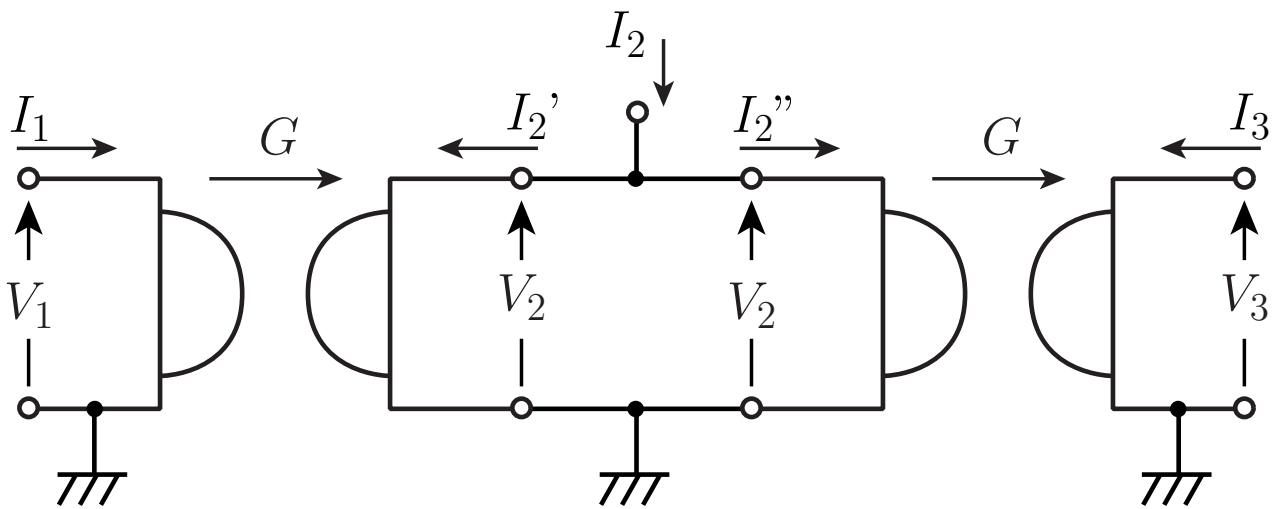
$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} 0 & \pm G \\ \mp G & 0 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$$

$$I_1 = \pm G V_2 = \pm G(-Z_L I_2) = \pm G(\pm Z_L G V_1) = Z_L G^2 V_1$$

$$\boxed{Z_{in} = \frac{V_1}{I_1} = \frac{1}{G^2 Z_L}}$$

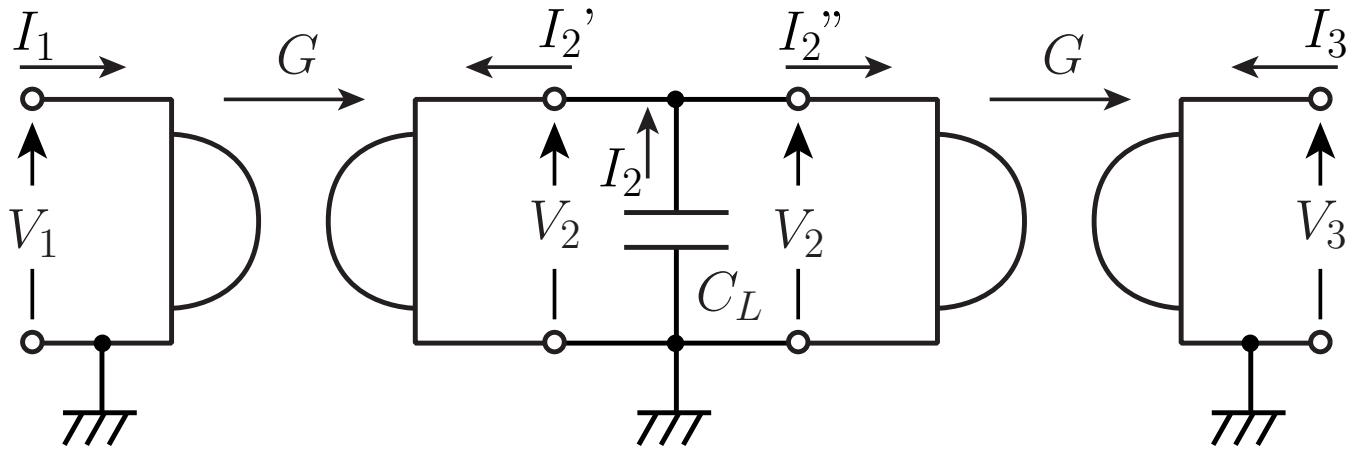
$$\boxed{Z_L = \frac{1}{sC_L} \rightarrow Z_{in} = s\frac{C_L}{G^2} \quad \left(L = \frac{C_L}{G^2}\right)}$$

Floating Inductor Simulation using 3-port Gyrator



$$\begin{bmatrix} I_1 \\ I_2' \end{bmatrix} = \begin{bmatrix} 0 & \pm G \\ \mp G & 0 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \qquad \begin{bmatrix} I_2'' \\ I_3 \end{bmatrix} = \begin{bmatrix} 0 & \pm G \\ \mp G & 0 \end{bmatrix} \begin{bmatrix} V_2 \\ V_3 \end{bmatrix}$$

$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = \begin{bmatrix} I_1 \\ I_2'+I_2'' \\ I_3 \end{bmatrix} = \begin{bmatrix} 0 & \pm G & 0 \\ \mp G & 0 & \pm G \\ 0 & \mp G & 0 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix}$$



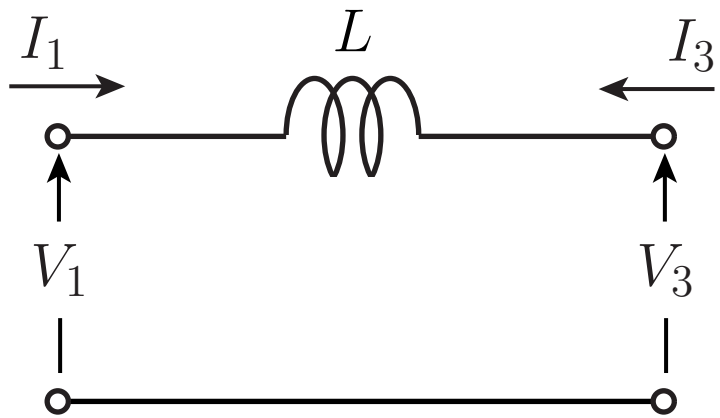
$$I_2 = -sC_L V_2$$

$$I_2 = \mp G(V_1 - V_3)$$

$$\longrightarrow \quad V_2 = \pm \frac{V_1 - V_3}{sC_L}$$

$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = \begin{bmatrix} 0 & \pm G & 0 \\ \mp G & 0 & \pm G \\ 0 & \mp G & 0 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} \longrightarrow \begin{bmatrix} I_1 \\ I_3 \end{bmatrix} = \begin{bmatrix} \frac{G^2}{sC_L} & -\frac{G^2}{sC_L} \\ -\frac{G^2}{sC_L} & \frac{G^2}{sC_L} \end{bmatrix} \begin{bmatrix} V_1 \\ V_3 \end{bmatrix}$$

$$\boxed{I_1 = -I_3}$$



$$\begin{bmatrix} I_1 \\ I_3 \end{bmatrix} = \begin{bmatrix} \frac{1}{sL} & -\frac{1}{sL} \\ -\frac{1}{sL} & \frac{1}{sL} \end{bmatrix} \begin{bmatrix} V_1 \\ V_3 \end{bmatrix}$$

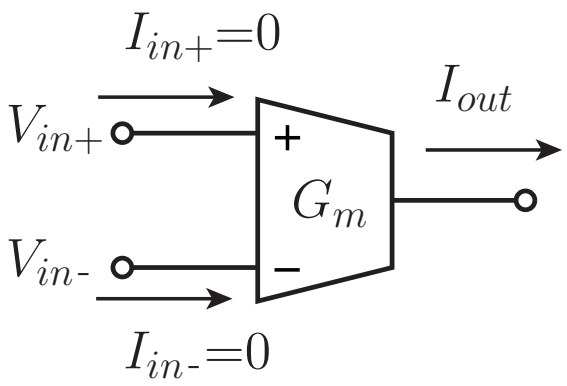
Y matrix for floating inductor

$$\begin{bmatrix} I_1 \\ I_3 \end{bmatrix} = \begin{bmatrix} \frac{G^2}{sC_L} & -\frac{G^2}{sC_L} \\ -\frac{G^2}{sC_L} & \frac{G^2}{sC_L} \end{bmatrix} \begin{bmatrix} V_1 \\ V_3 \end{bmatrix}$$

$$\boxed{L = \frac{C_L}{G^2}}$$

Gyrator Implementation using OTAs

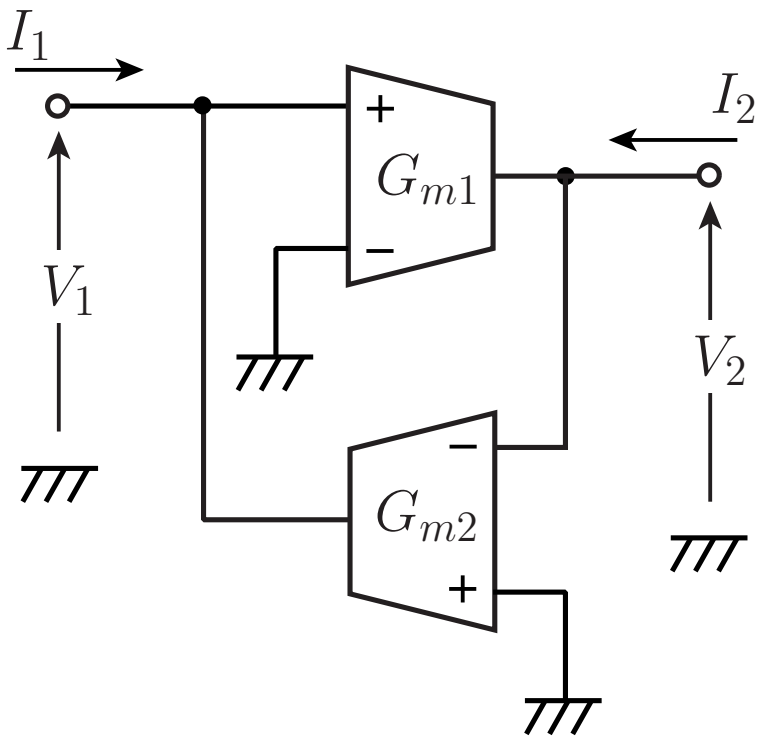
OTA: Operational Transconductance Amplifier



$$I_{out}=G_m(V_{in+}-V_{in-})$$

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} 0 & G \\ -G & 0 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$$

Y matrix for gyrator

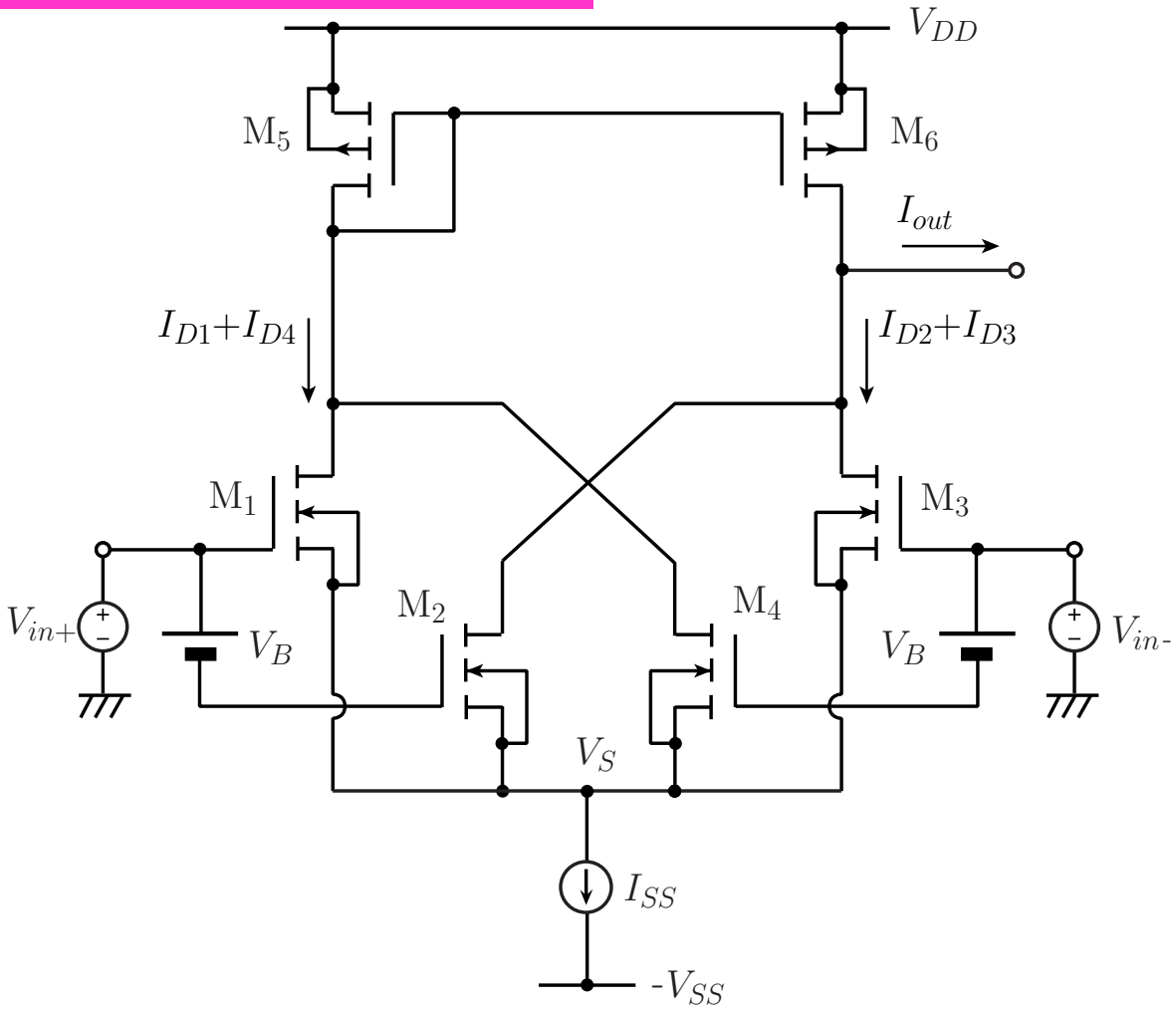


$$I_1 = -G_{m2}(0 - V_2) = G_{m2}V_2$$

$$I_2 = -G_{m1}(V_1 - 0) = G_{m1}V_1$$

$$G_{m1} = G_{m2} = G$$

OTA Implementation Example



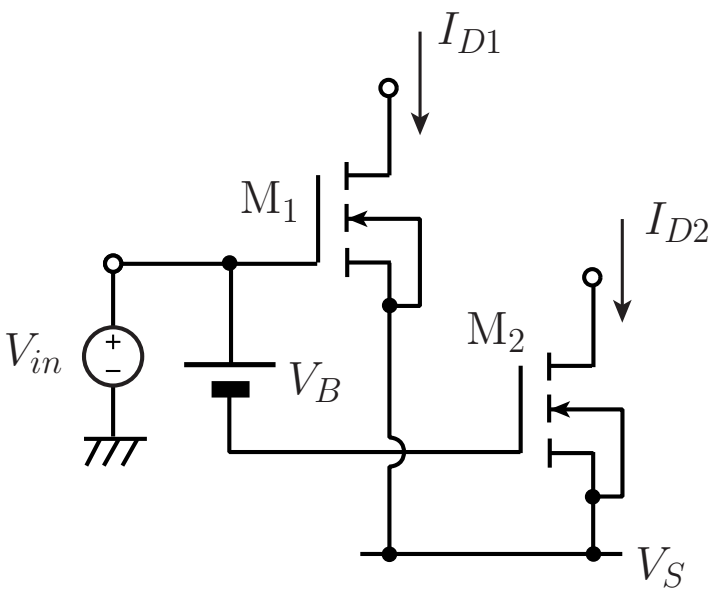
$$I_{out}=(I_{D1}+I_{D4})-(I_{D2}+I_{D3})=2KV_B(V_{in+}-V_{in-})$$

$2KV_B$: transconductance

Bias Offset Technique

Square Law : $I_D = K(V_{GS} - V_T)^2$

$$K = \frac{1}{2}\mu C_{OX}\frac{W}{L}$$



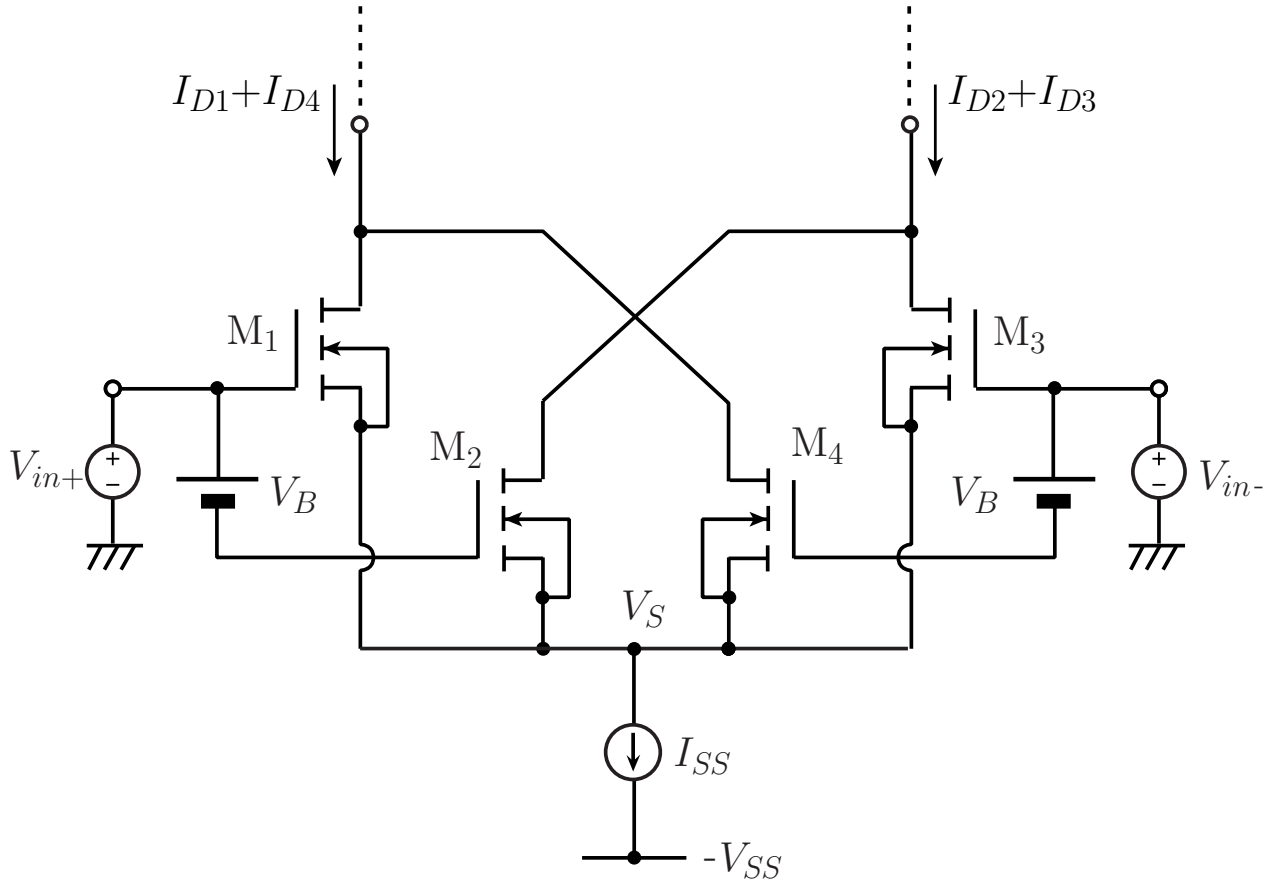
$$I_{D1} = K(V_{in} - V_S - V_T)^2$$

$$I_{D2} = K(V_{in} - V_B - V_S - V_T)^2$$

$$I_{D1} - I_{D2} = K(2V_{in} - V_B - 2V_S - 2V_T)V_B$$

$$= 2KV_BV_{in} - K(V_B + 2V_S + 2V_T)V_B$$

Offset Currents Cancellation

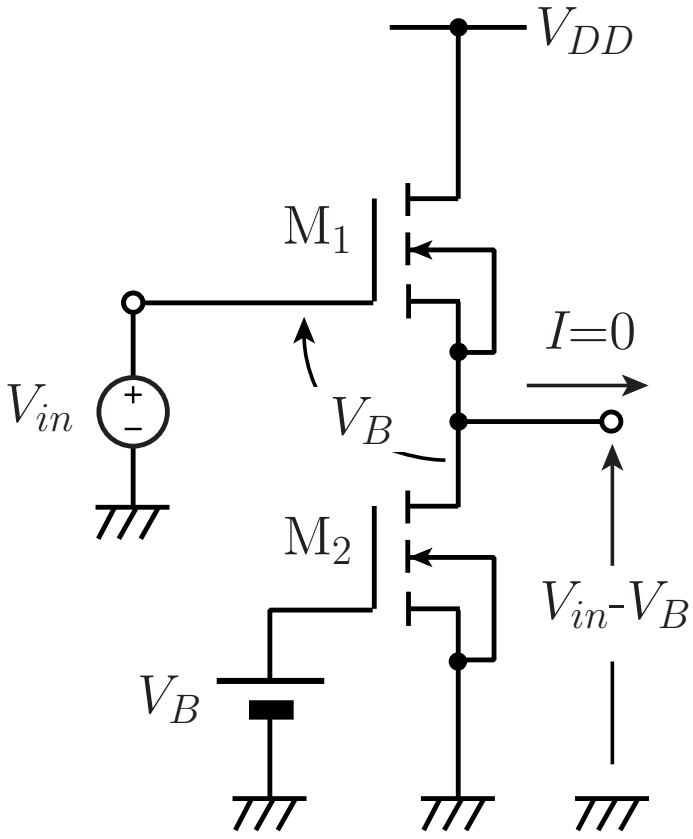


$$I_{D1}-I_{D2}=2KV_BV_{in+}-K(V_B+2V_S+2V_T)V_B$$

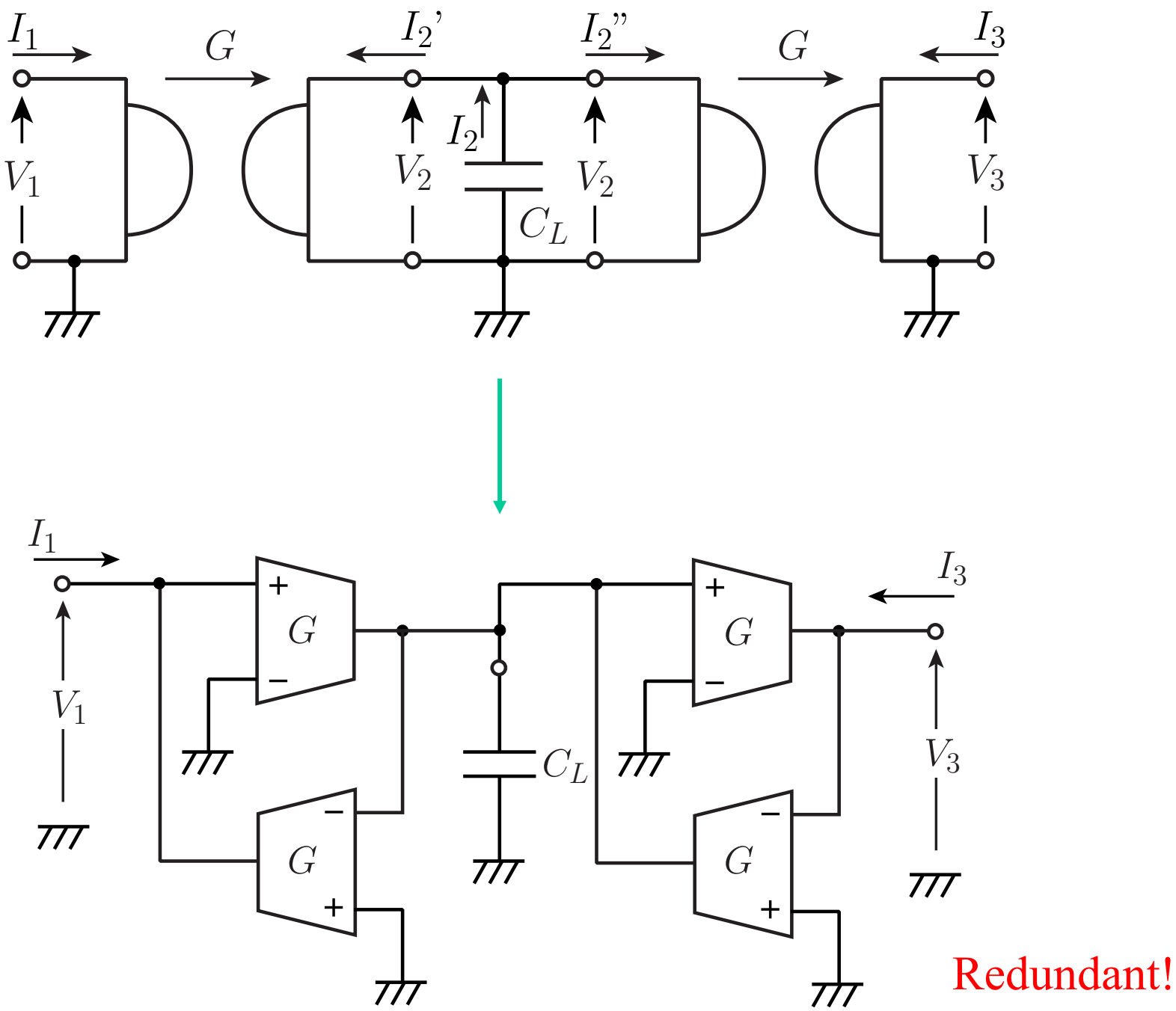
$$I_{D3}-I_{D4}=2KV_BV_{in-}-K(V_B+2V_S+2V_T)V_B$$

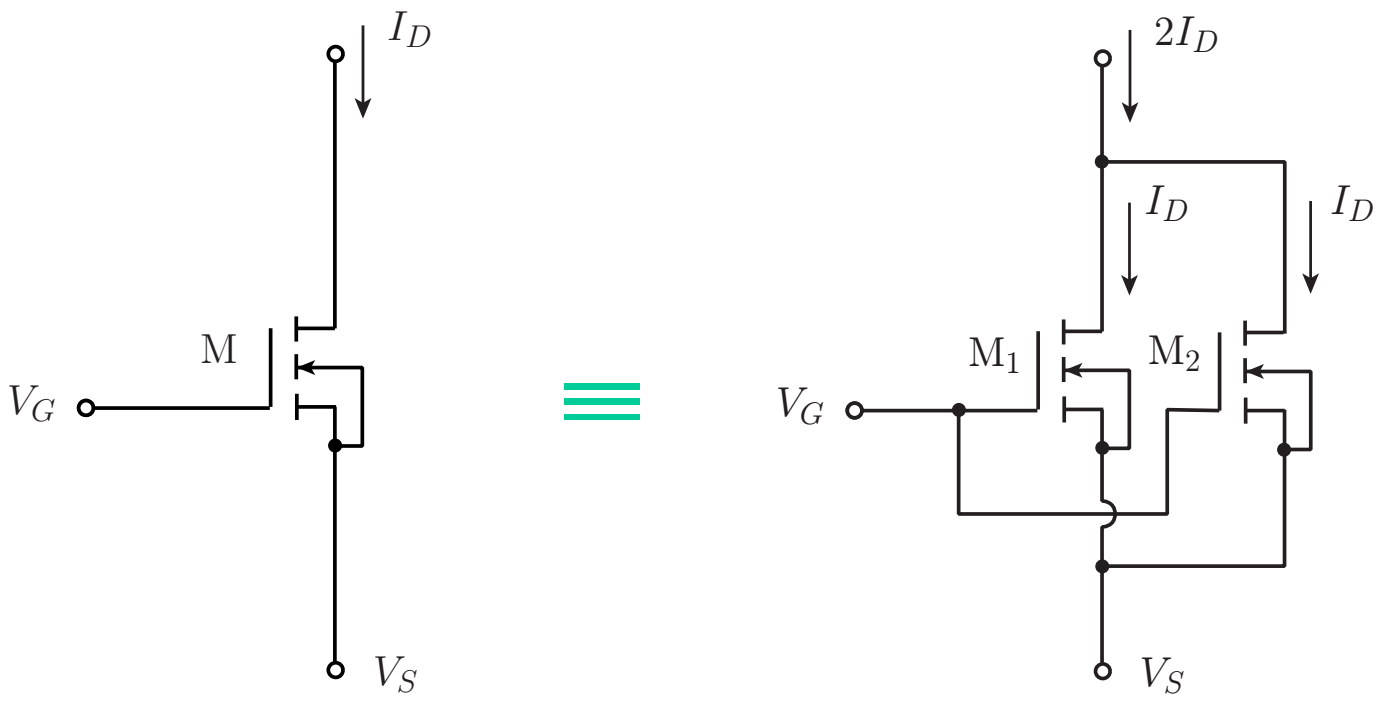
$$\boxed{\begin{aligned}I_{out}&=(I_{D1}+I_{D4})-(I_{D2}+I_{D3})=(I_{D1}-I_{D2})-(I_{D3}-I_{D4})\\&=2KV_B(V_{in+}-V_{in-})\end{aligned}}$$

Equivalent DC Voltate Source



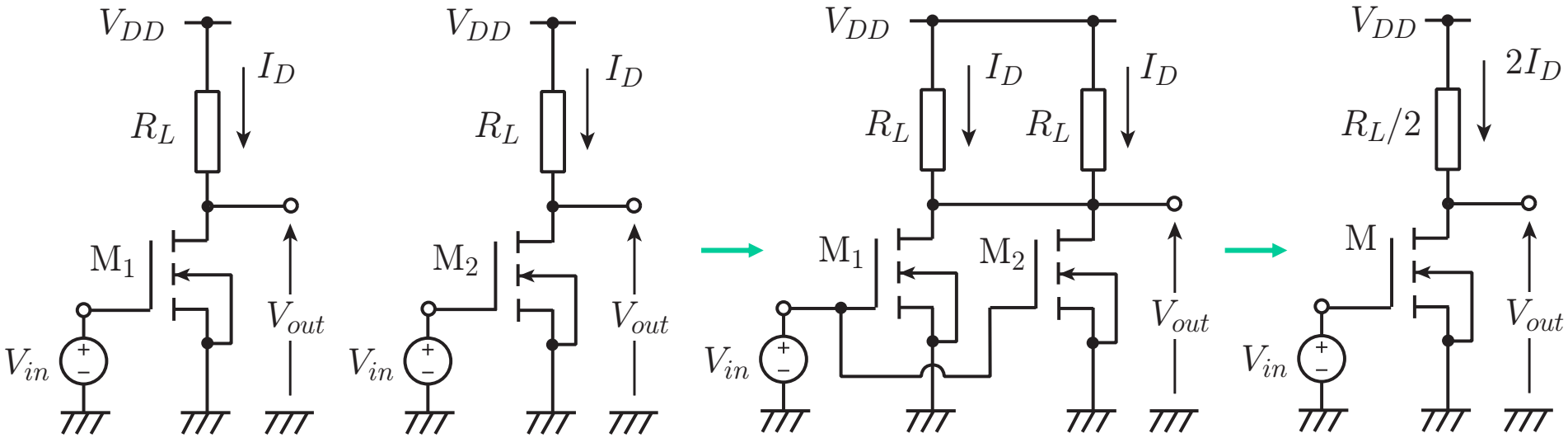
Square Law : $I_D = K(V_{GS} - V_T)^2$


I_1
G
I_2'
I_2"
G
I_3
V_1
V_2
I_2
C_L
V_2
V_3
I_1
G
G
C_L
G
G
I_3
V_1
V_3
Redundant!



$$I_D = K(V_{GS} - V_T)^2 \qquad 2I_D = 2K(V_{GS} - V_T)^2$$

$$\boxed{K = \frac{1}{2}\mu C_{OX}\frac{W}{L}}$$



M_1: K, I_D

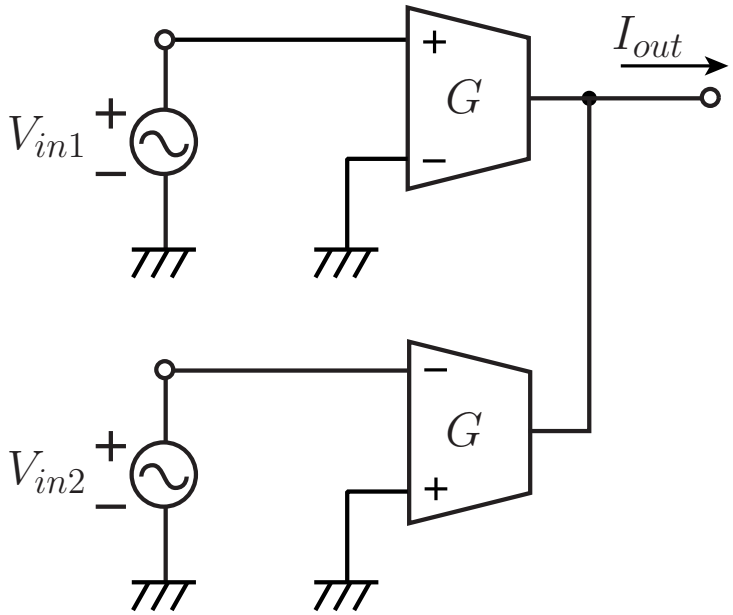
M_2: K, I_D

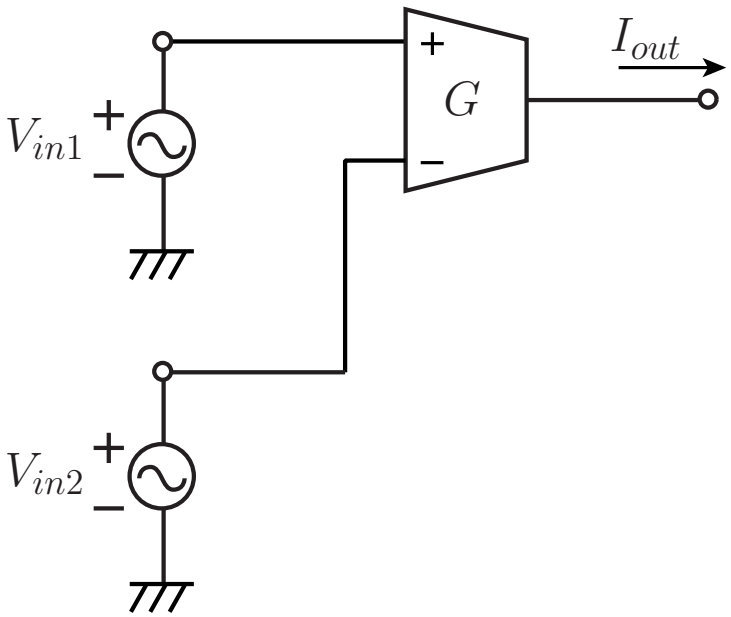
$\boxed{M : 2K, \ 2I_D}$

$2KV_B$: transconductance

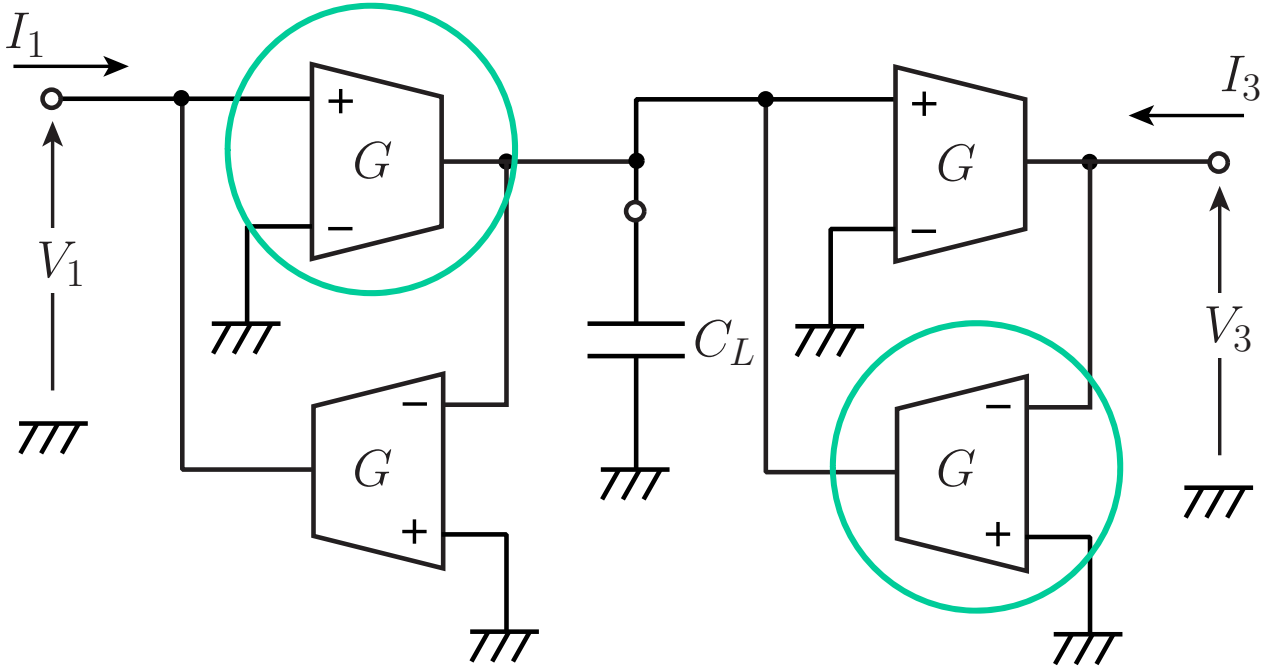
Power and chip area are proportional to transconductance!

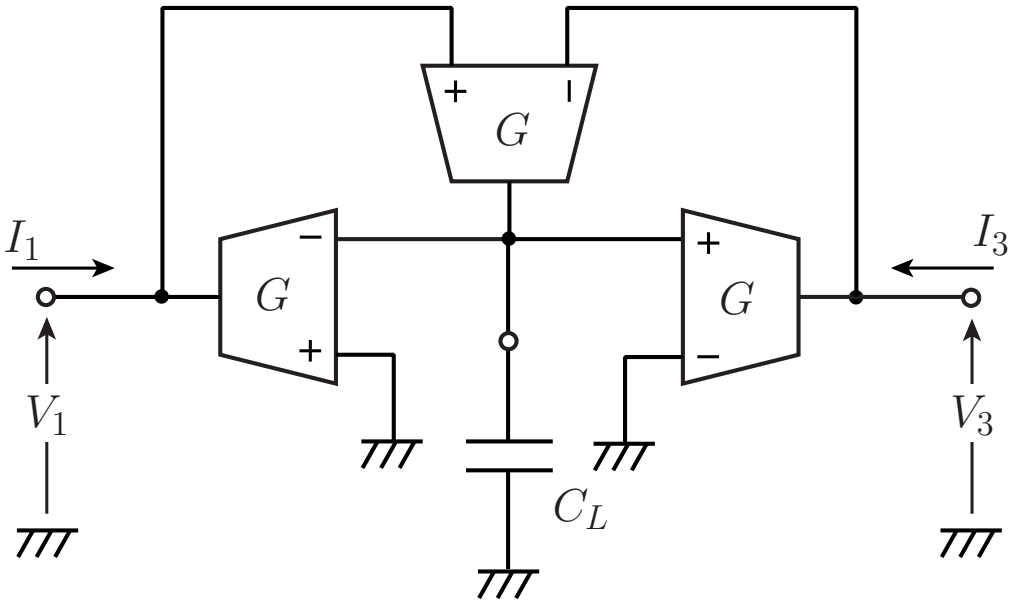
OTA Sharing Technique



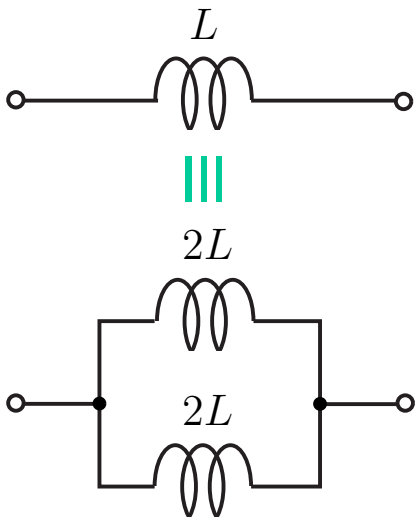


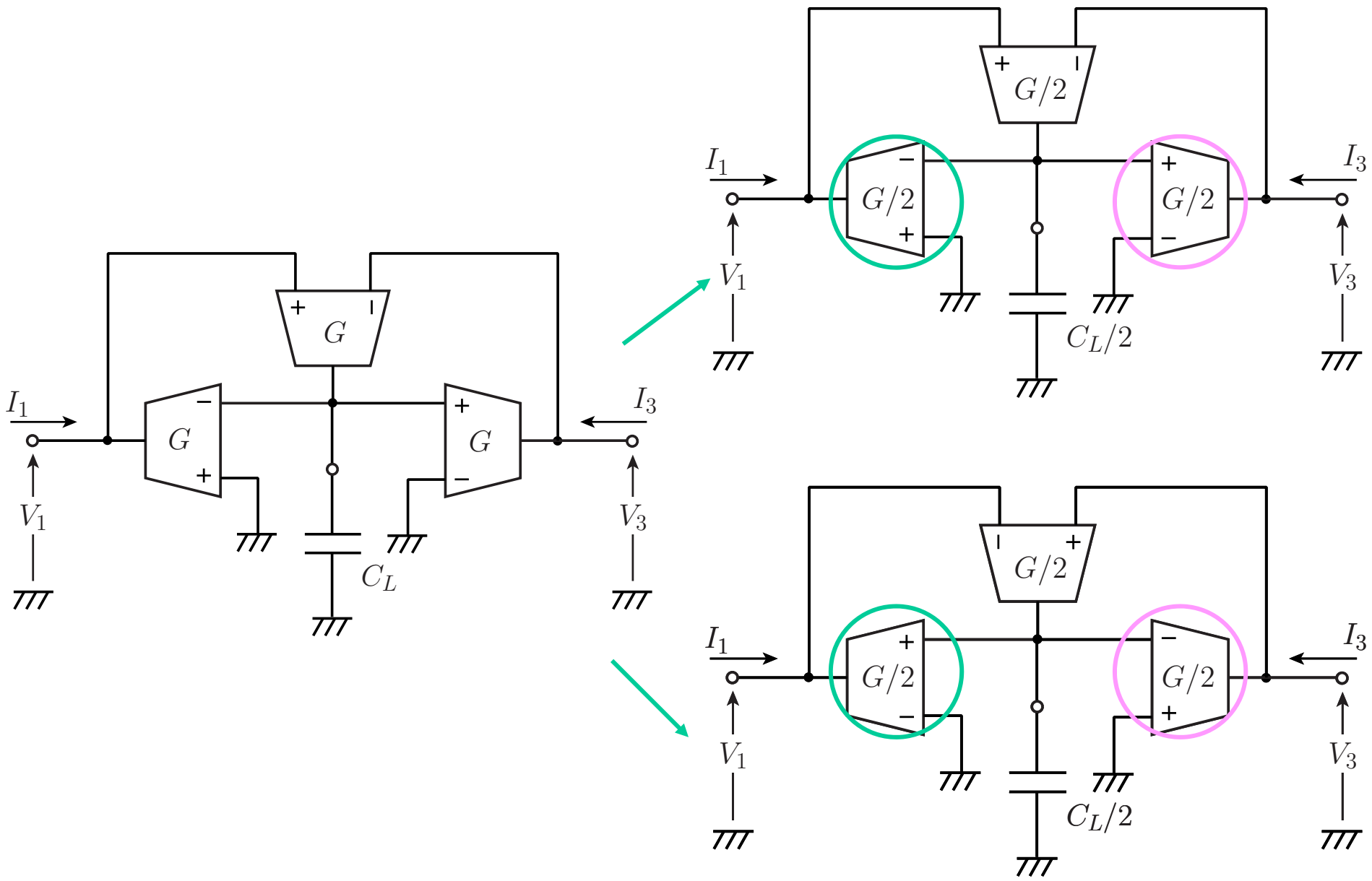
$$I_{out}=G(V_{in1}-V_{in2})$$

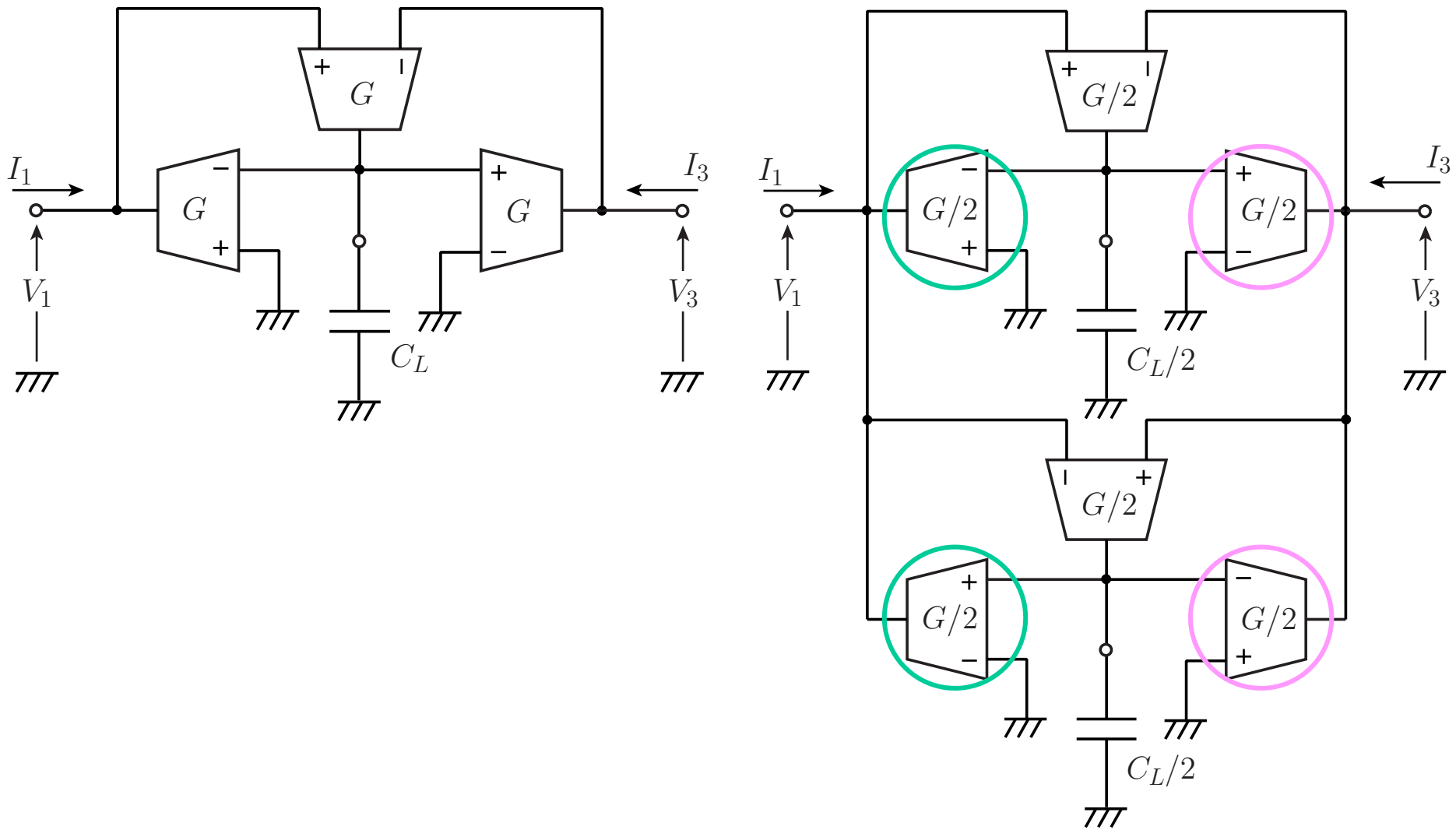

I_1
V_1
G
G
C_L
G
G
I_3
V_3

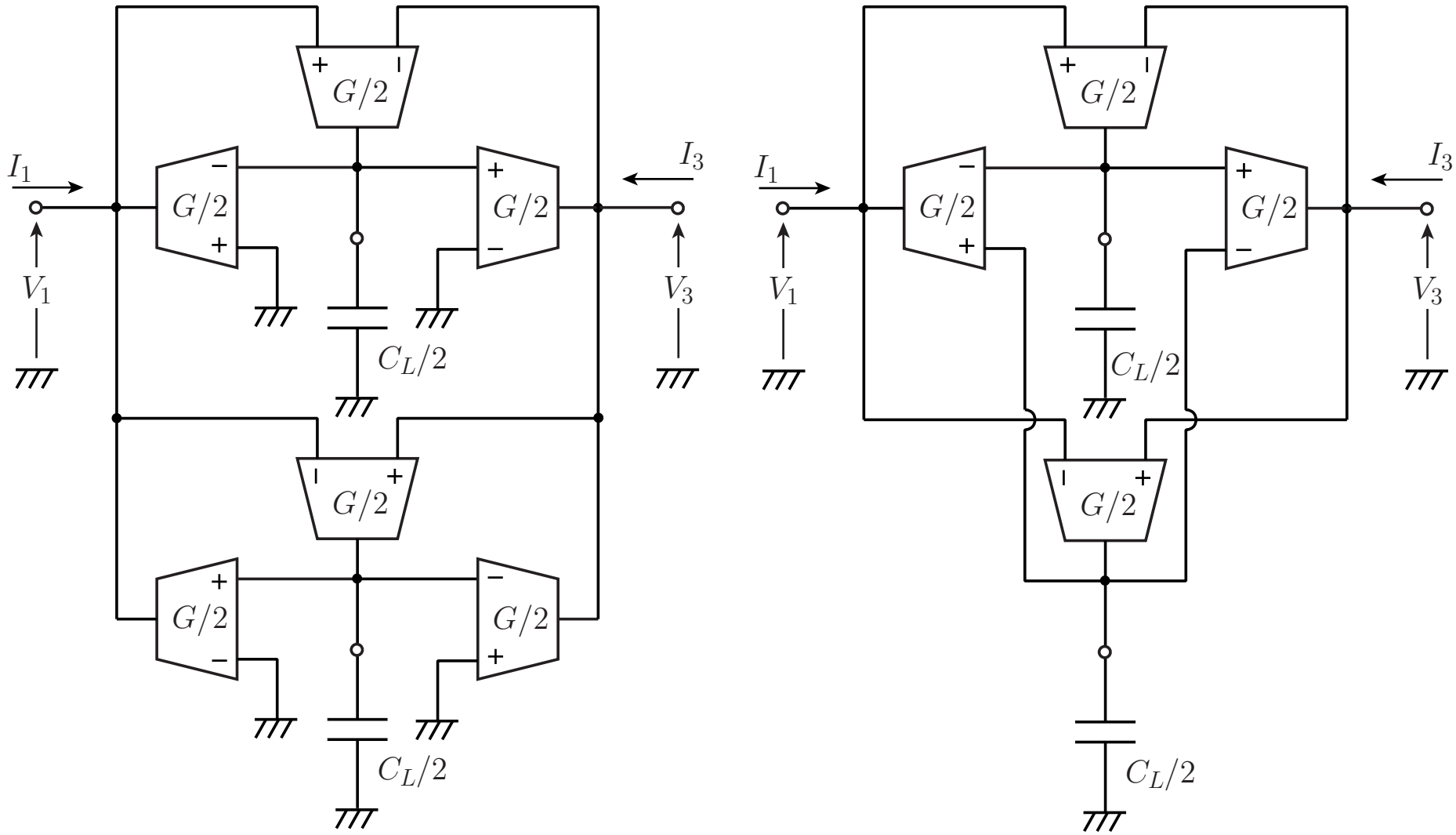

G
I_1
V_1
G
G
C_L
I_3
V_3

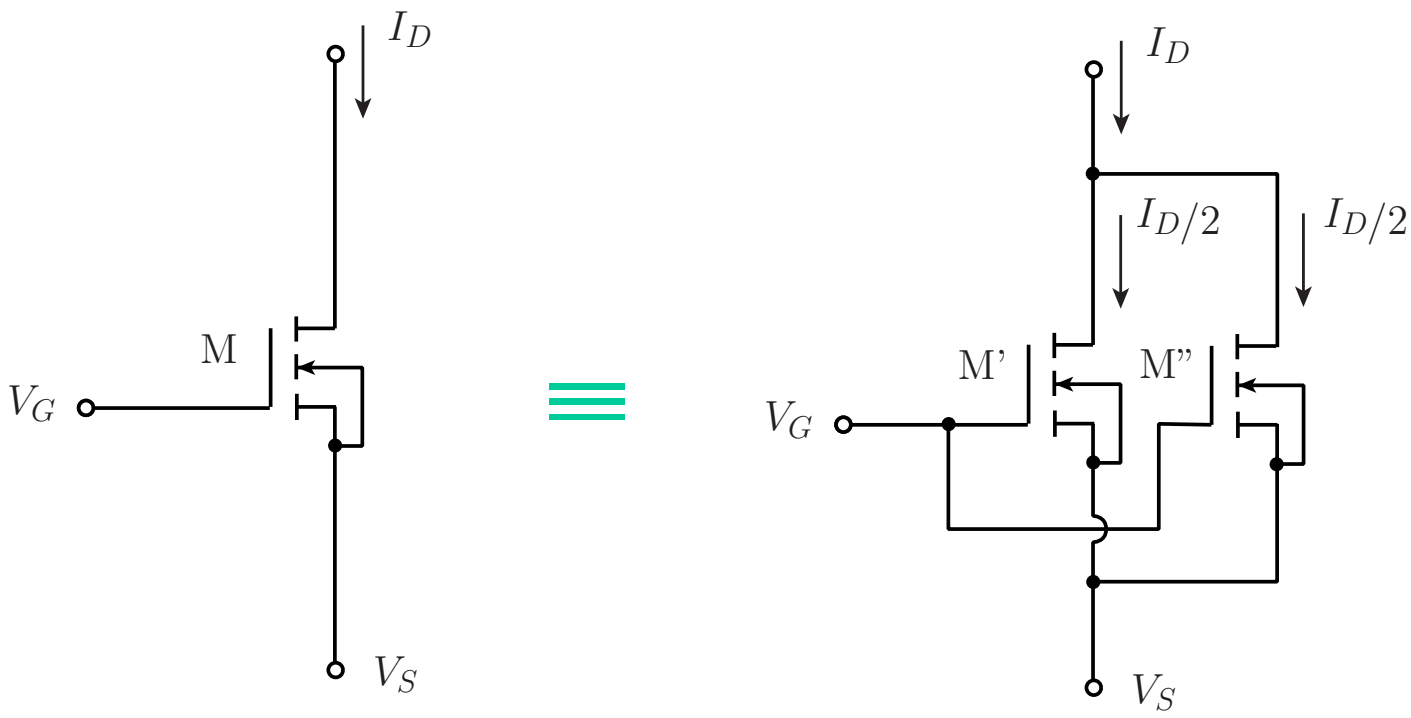
Inductor Dividing Technique




I_1
V_1
G
G
G
C_L
I_3
V_3
$G/2$
$G/2$
$G/2$
$C_L/2$
$G/2$
$G/2$
$G/2$
$C_L/2$

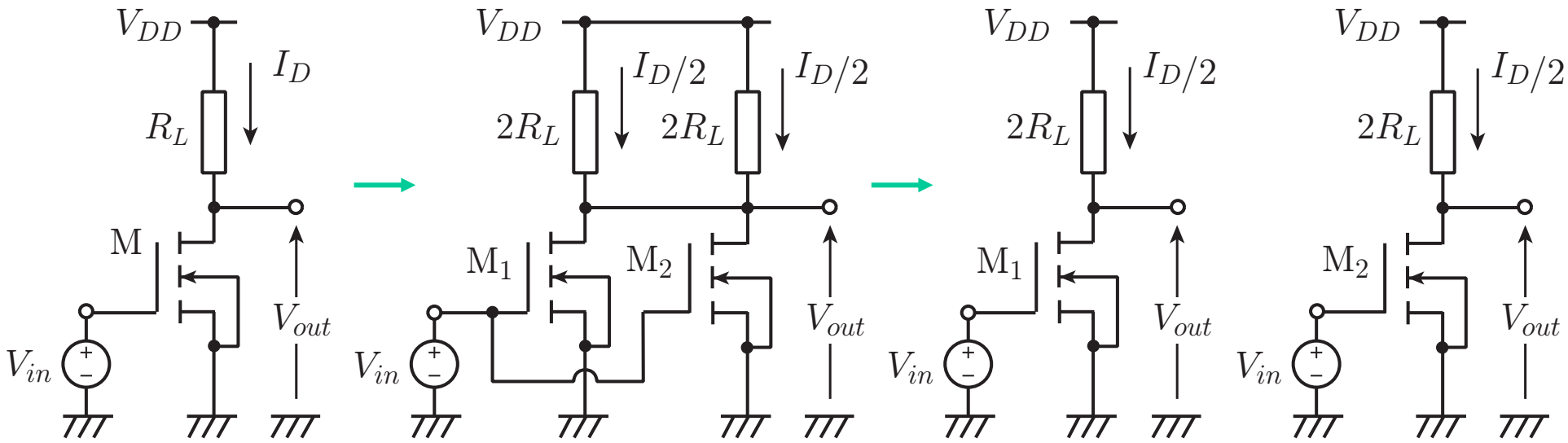

I_1
V_1
G
G
G
C_L
I_3
V_3
I_1
V_1
$G/2$
$G/2$
$G/2$
$C_L/2$
$G/2$
$G/2$
$G/2$
$C_L/2$
I_3
V_3


I_1
V_1
$G/2$
$G/2$
$G/2$
$G/2$
$C_L/2$
I_3
V_3
$G/2$
$G/2$
$G/2$
$G/2$
$C_L/2$
I_1
V_1
$G/2$
$G/2$
$G/2$
$C_L/2$
I_3
V_3
$C_L/2$



$$I_D = K(V_{GS} - V_T)^2 \qquad I_D/2 = \frac{K}{2}(V_{GS} - V_T)^2$$

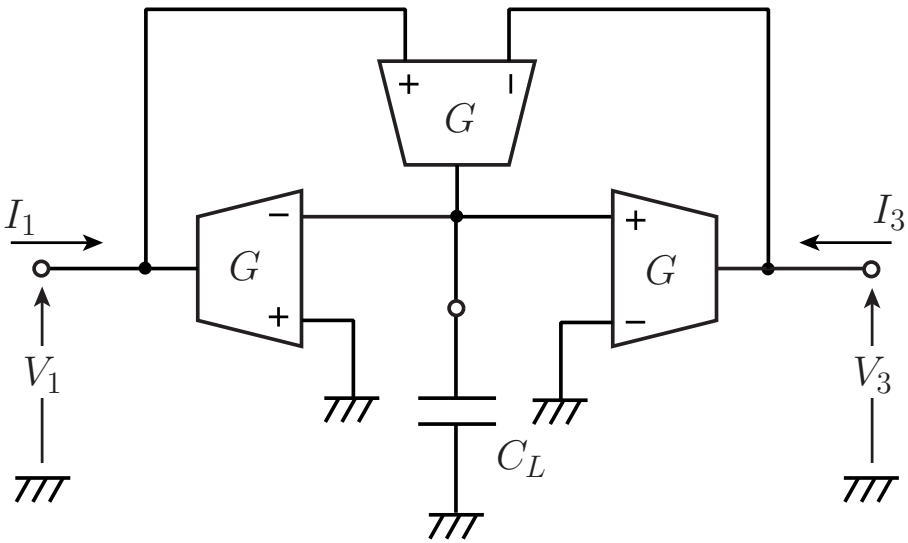
$$\boxed{K = \frac{1}{2}\mu C_{OX}\frac{W}{L}}$$



$$\boxed{\mathrm{M}: K, \quad I_D}$$

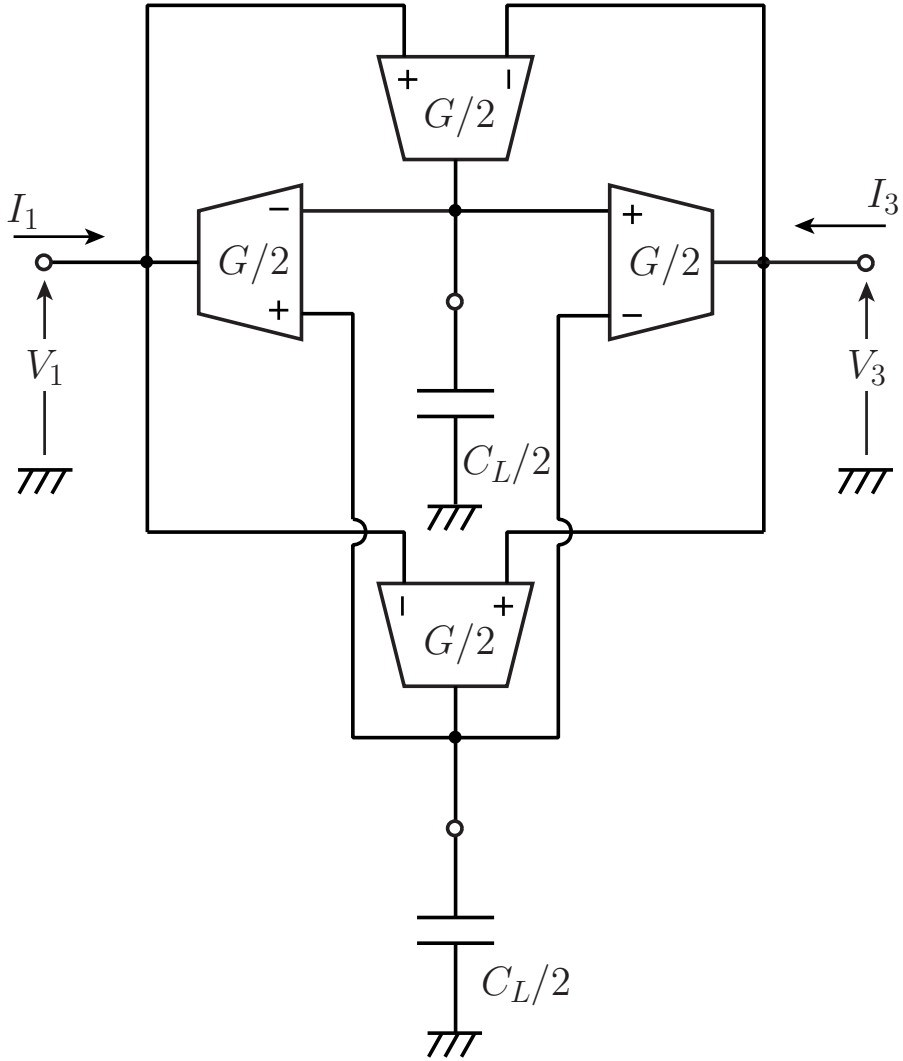
$$\boxed{\mathrm{M}_1: \frac{K}{2}, \quad \frac{I_D}{2}}$$

$$\boxed{\mathrm{M}_2: \frac{K}{2}, \quad \frac{I_D}{2}}$$



Chip Area : 3

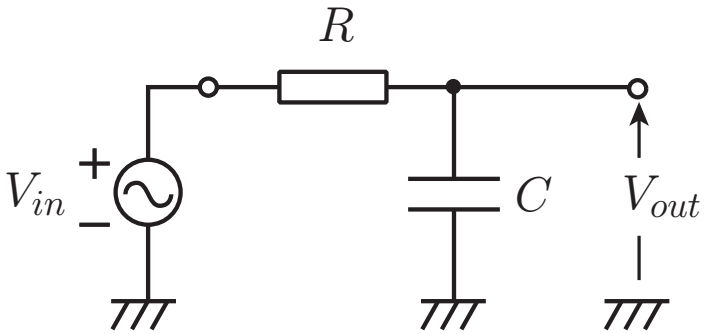
DC Power : 3

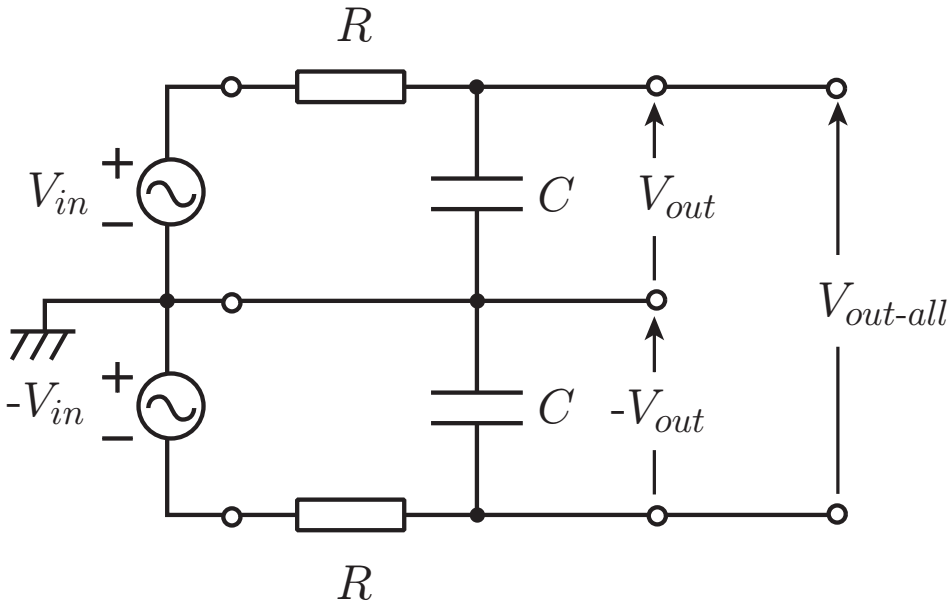


Chip Area : 2

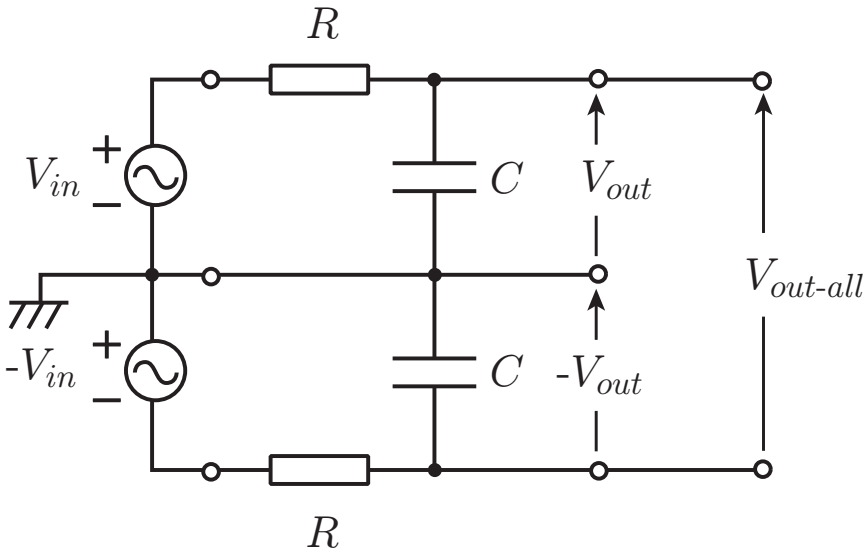
DC Power : 2

Balanced-Type Circuit





What is a merit?



Element Nonlinearity

$$V_{out}=a_0+a_1V_{in}+a_2V_{in}^2+a_3V_{in}^3+\cdots$$

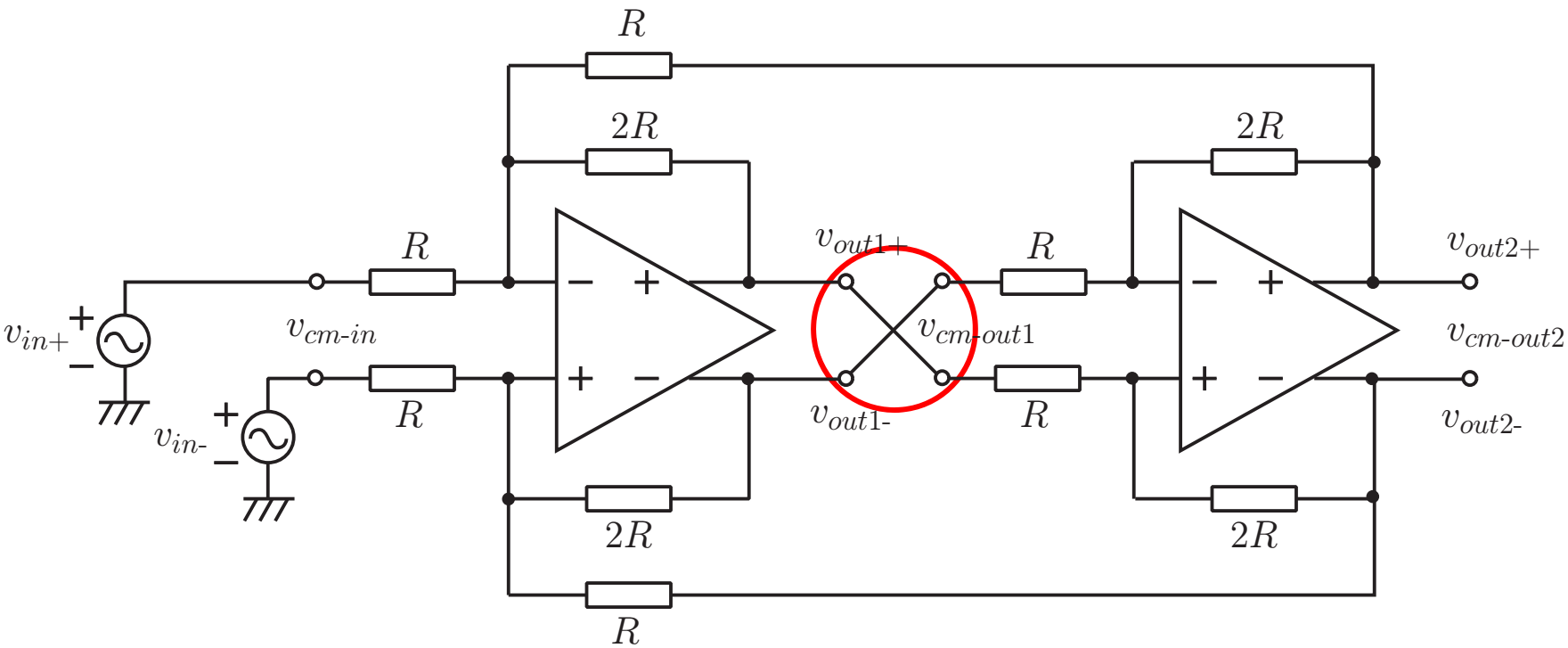
$$-V_{out}=a_0+a_1(-V_{in})+a_2V_{in}^2-a_3(-V_{in})^3+\cdots$$

$$=a_0-a_1V_{in}+a_2V_{in}^2-a_3V_{in}^3+\cdots$$

$$\boxed{V_{out\text{-}all}=V_{out}-(-V_{out})=2a_1V_{in}+2a_3V_{in}^3+\cdots}$$

Cancellation of Even-Order Distortions

What is a demerit?



differential-mode signal

$$v_{dif-in} = \frac{v_{in+} - v_{in-}}{2}$$

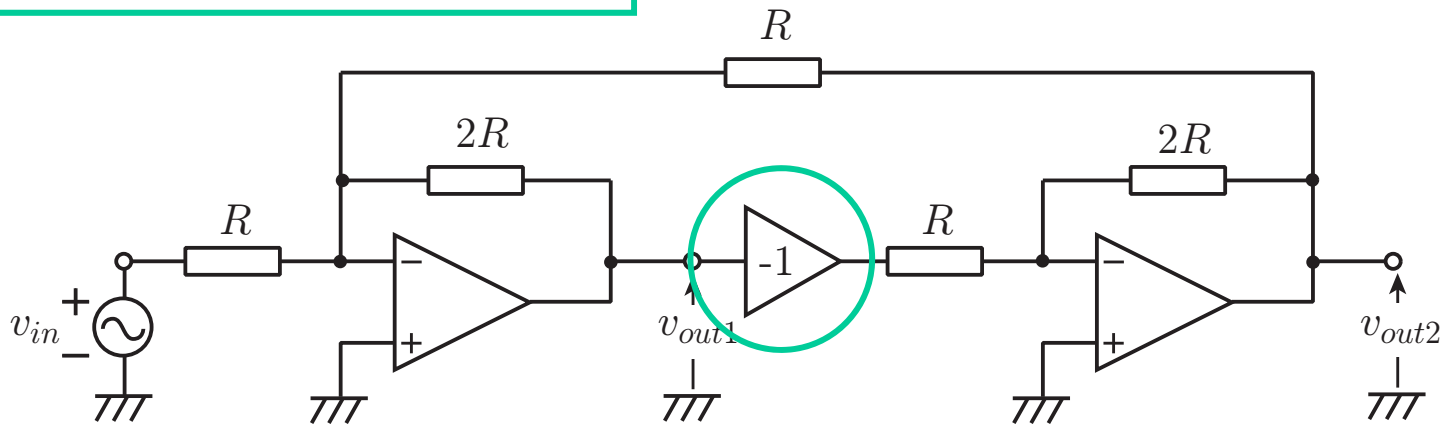
$$v_{in+} = v_{dif-in} + v_{cm-in}$$

common-mode signal

$$v_{cm-in} = \frac{v_{in+} + v_{in-}}{2}$$

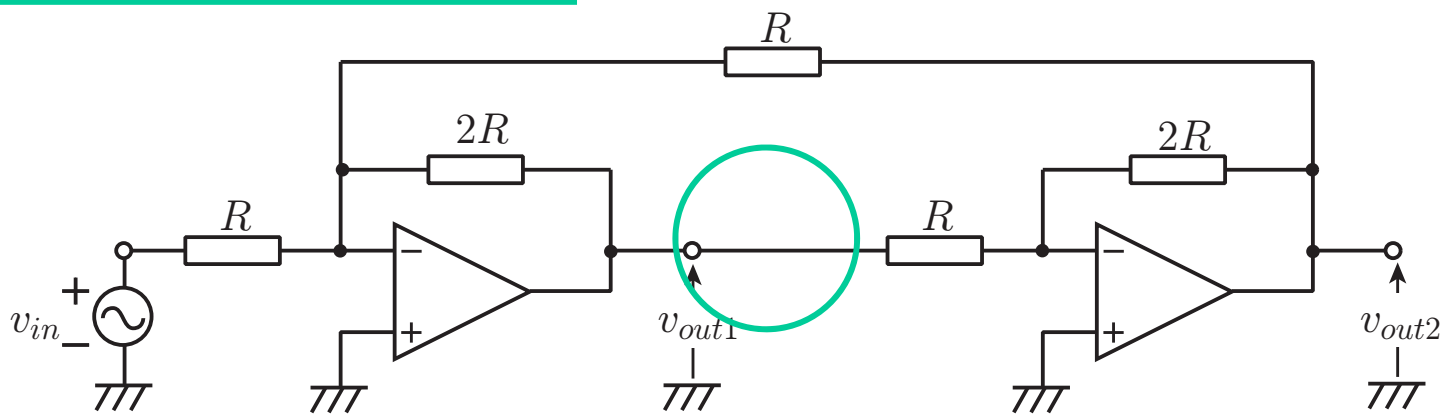
$$v_{in-} = -v_{dif-in} + v_{cm-in}$$

For differential-mode signals



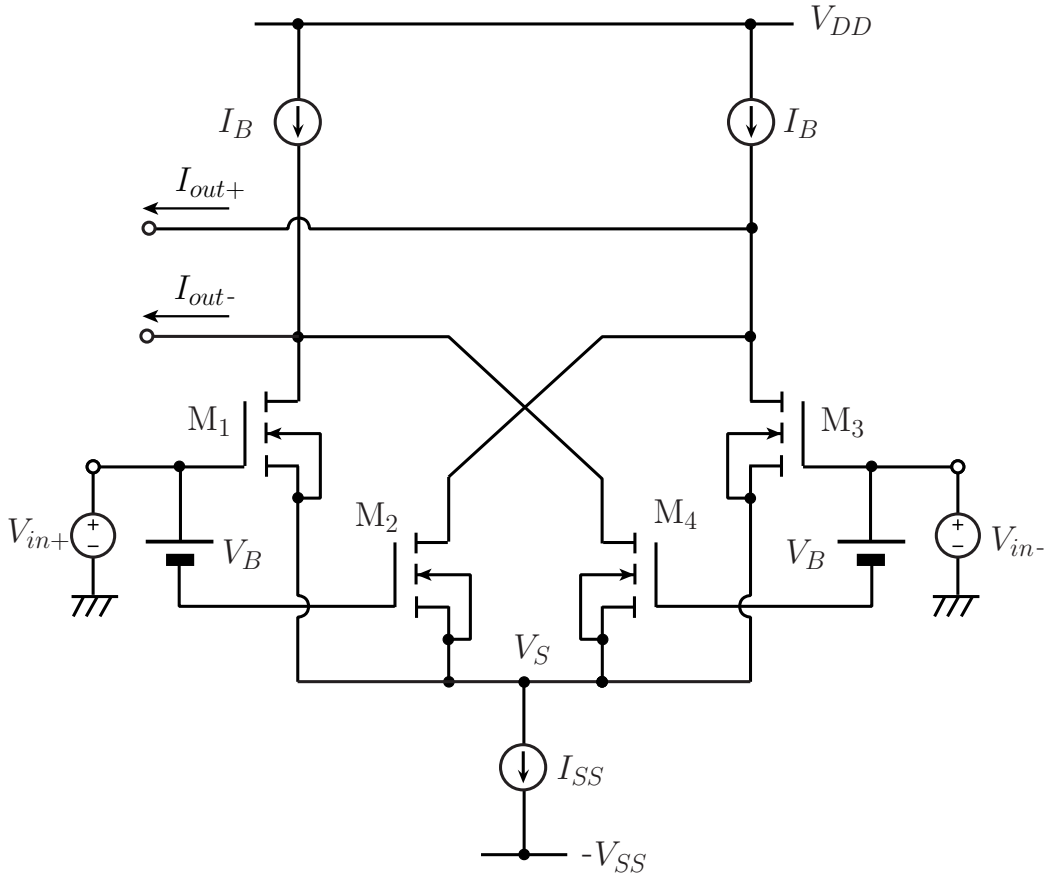
Negative Feedback: Stable

For common-mode signals

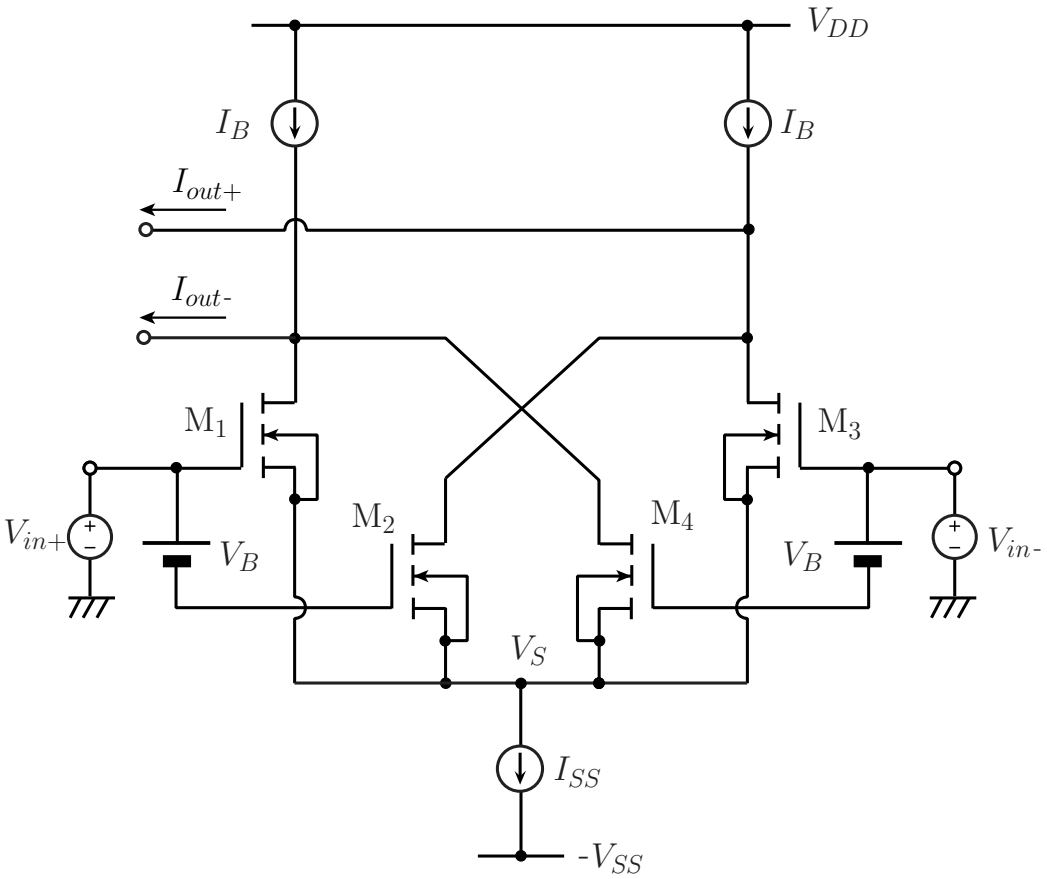


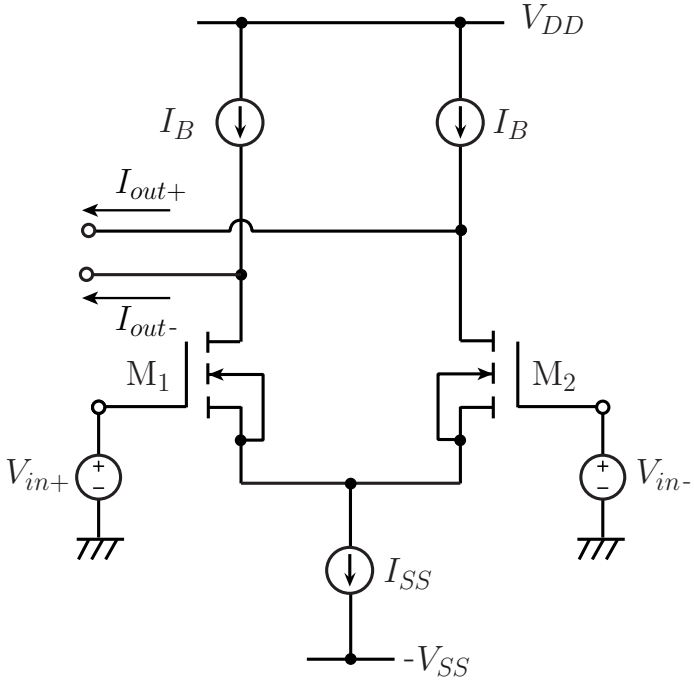
Positive Feedback: Unstable

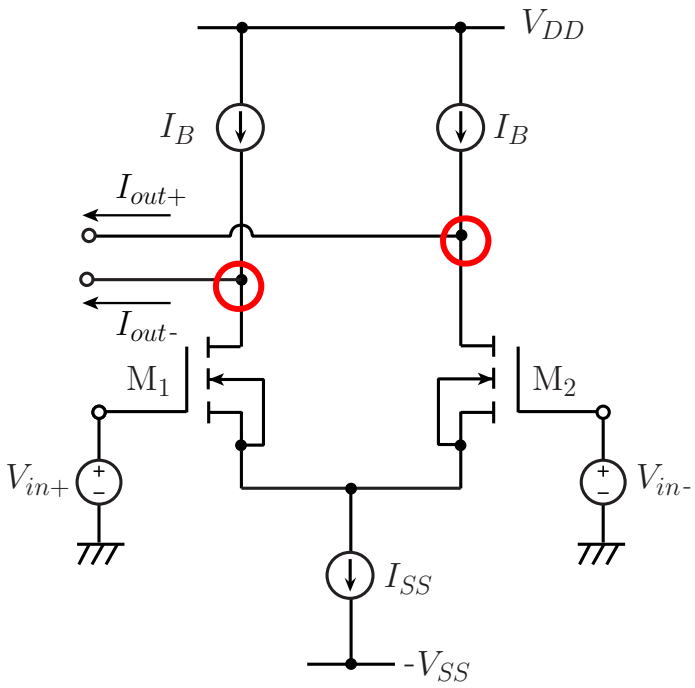
Balanced-Type OTA



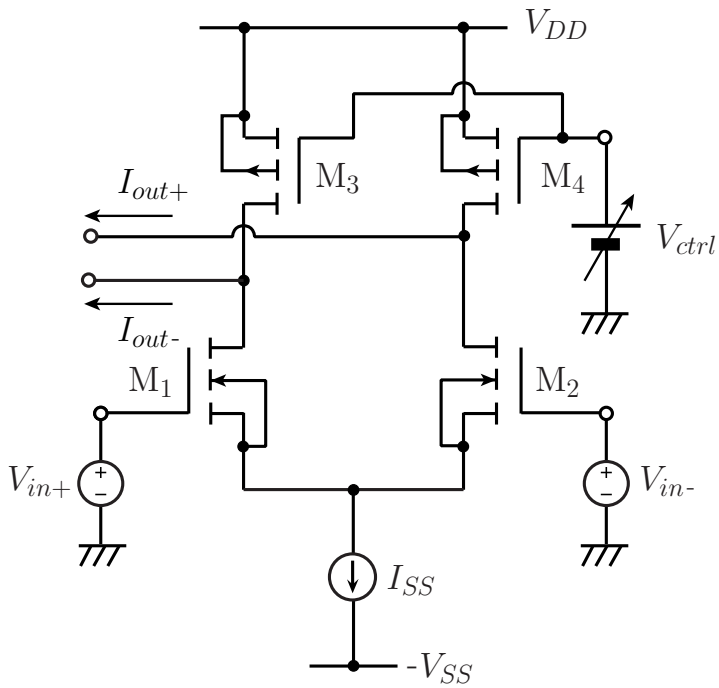
Bias Offset Technique Based


V_{DD}
I_B
I_B
I_{out+}
I_{out-}
M_1
M_3
V_{in+}
V_B
M_2
M_4
V_B
V_{in-}
V_S
I_{SS}
$-V_{SS}$

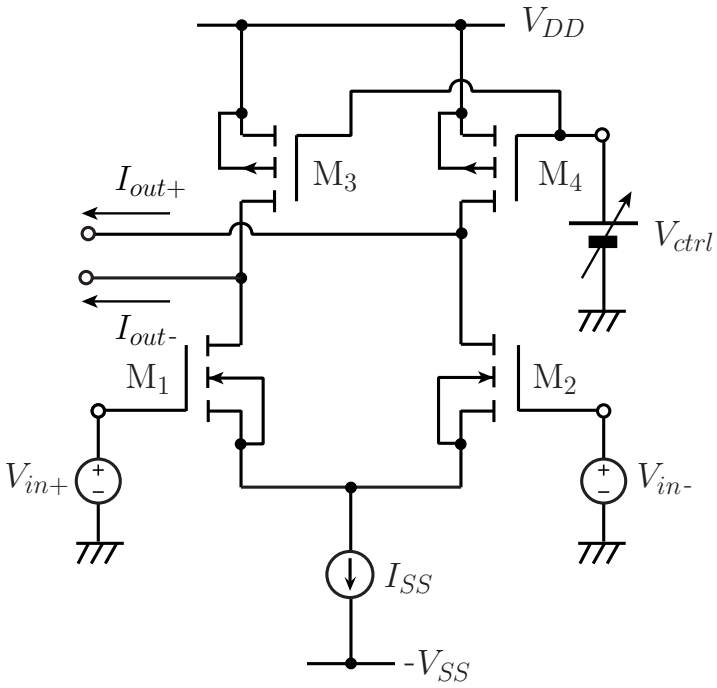

V_{DD}
I_B
I_B
I_{out+}
I_{out-}
M_1
M_2
V_{in+}
V_{in-}
I_{SS}
$-V_{SS}$



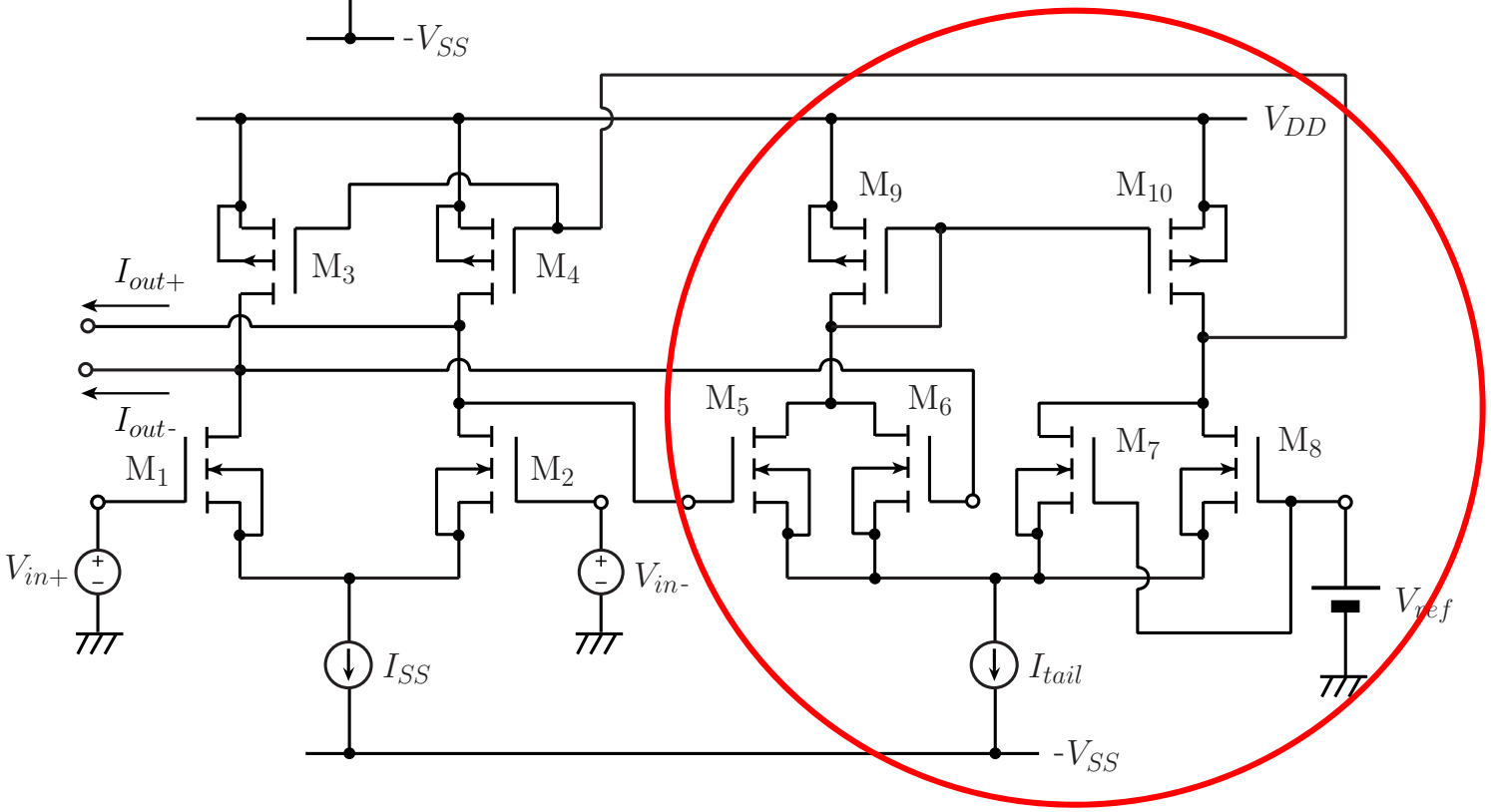
Unstable



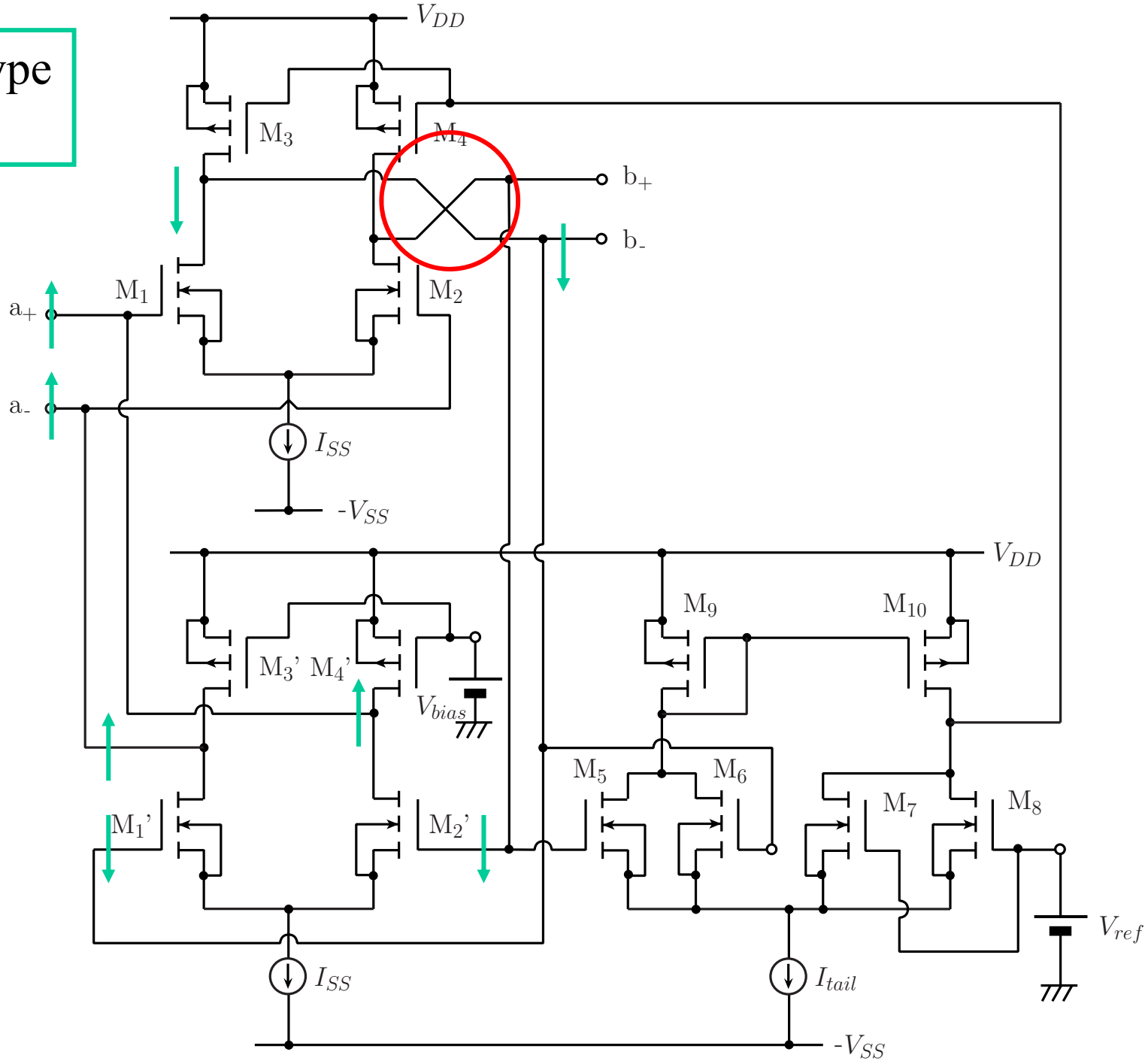
Stable by controlling
Current sources

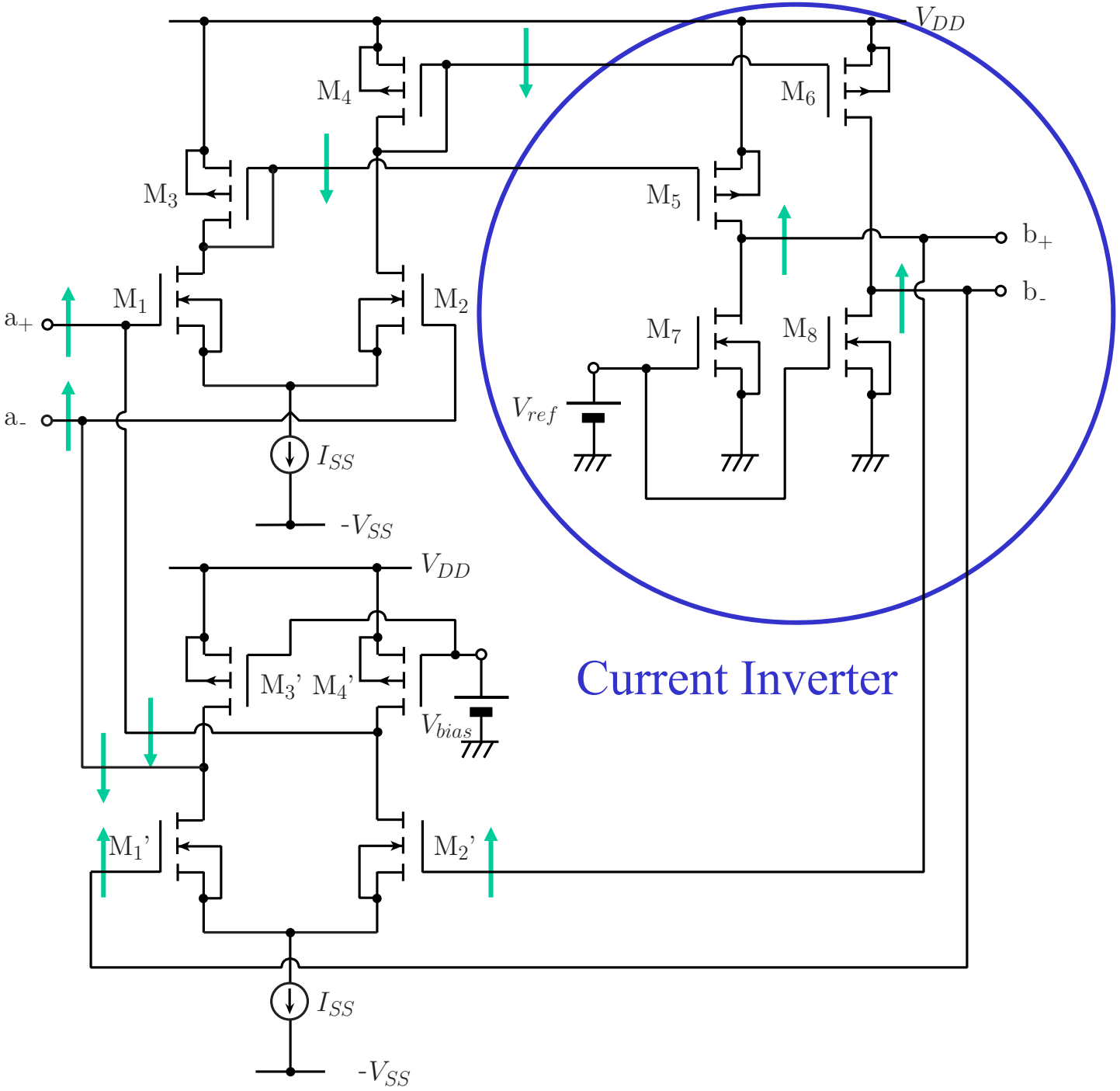


Common-Mode Feedback Circuit

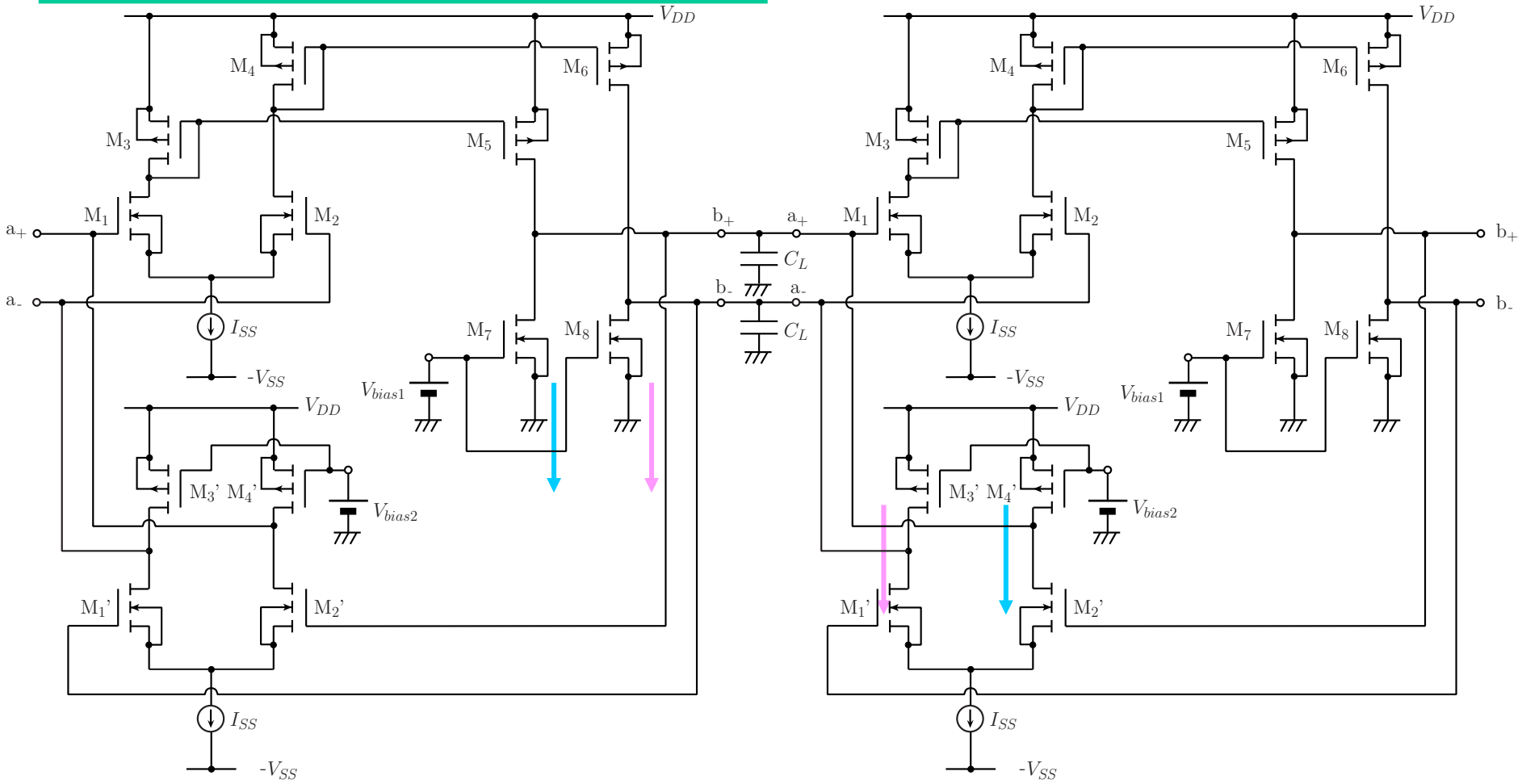


Balanced-Type Gyrator

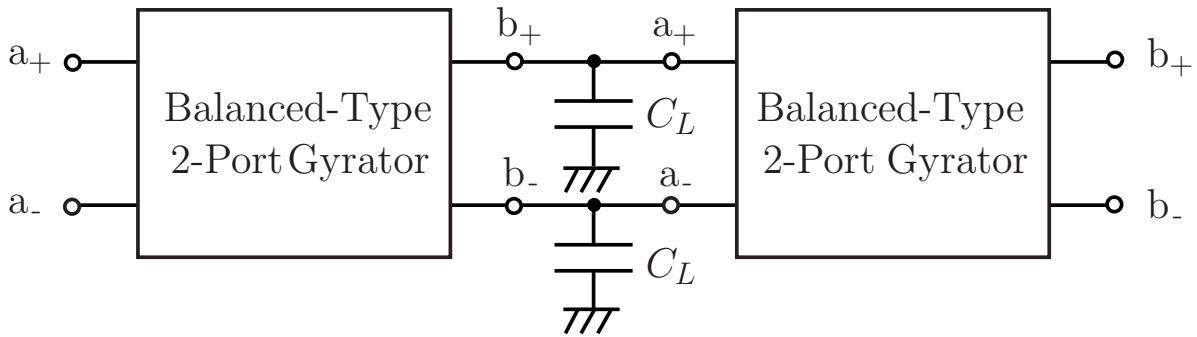



V_{DD}
M_4
M_6
M_3
M_5
b_+
b_-
M_1
M_2
a_+
M_7
M_8
a_-
V_{ref}
I_{SS}
$-V_{SS}$
V_{DD}
M_3' M_4'
V_{bias}
Current Inverter
M_1'
M_2'
I_{SS}
$-V_{SS}$

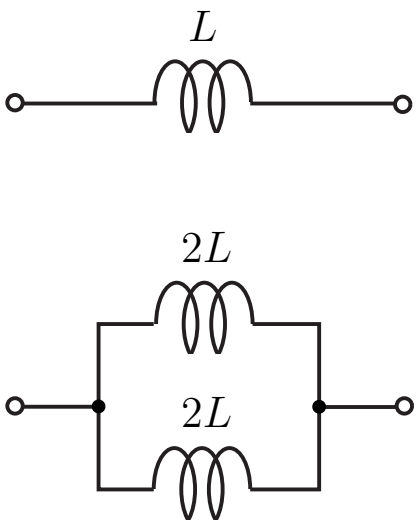
Balanced-Type Floating Inductor

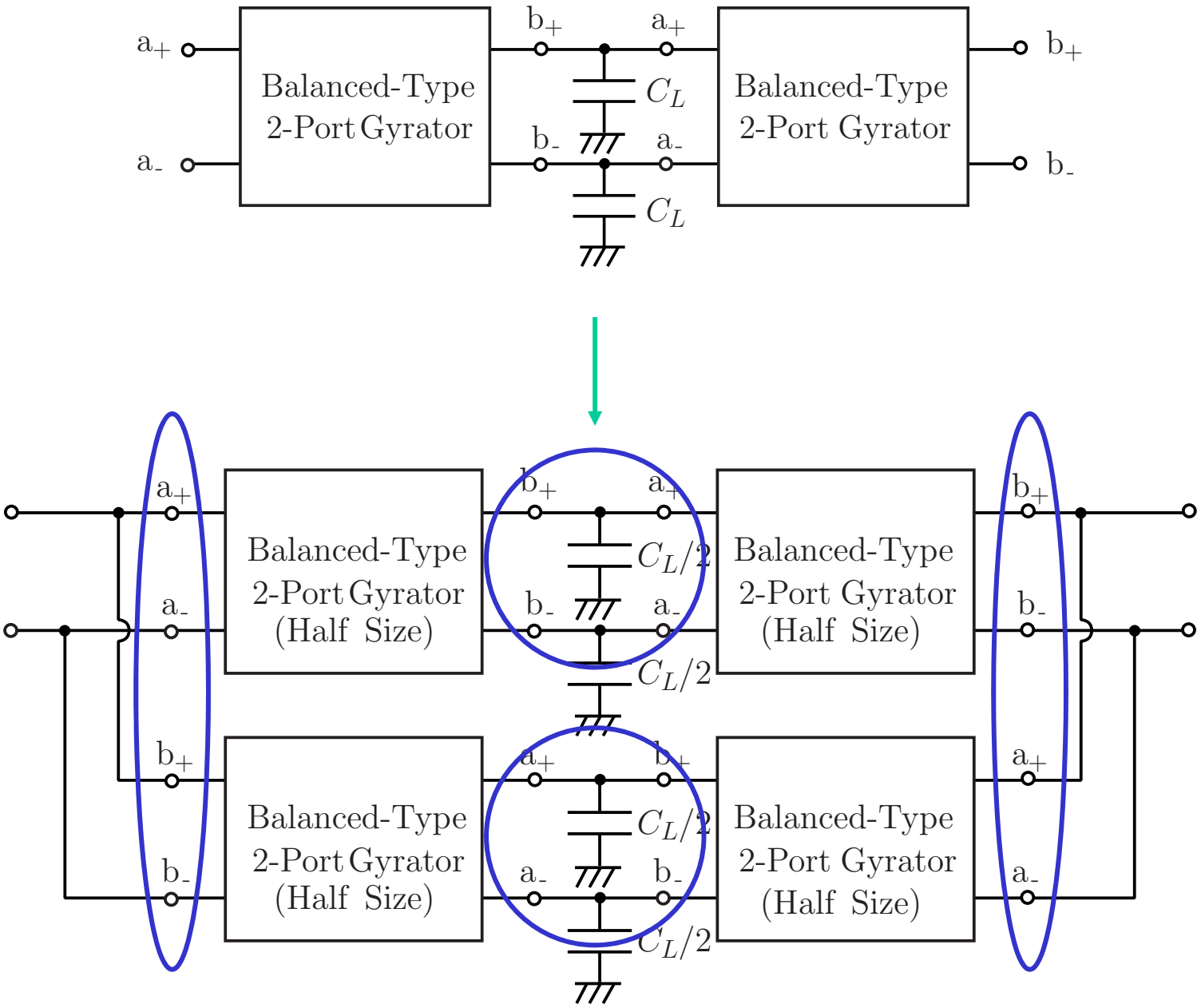


Current Source Cancelling Technique

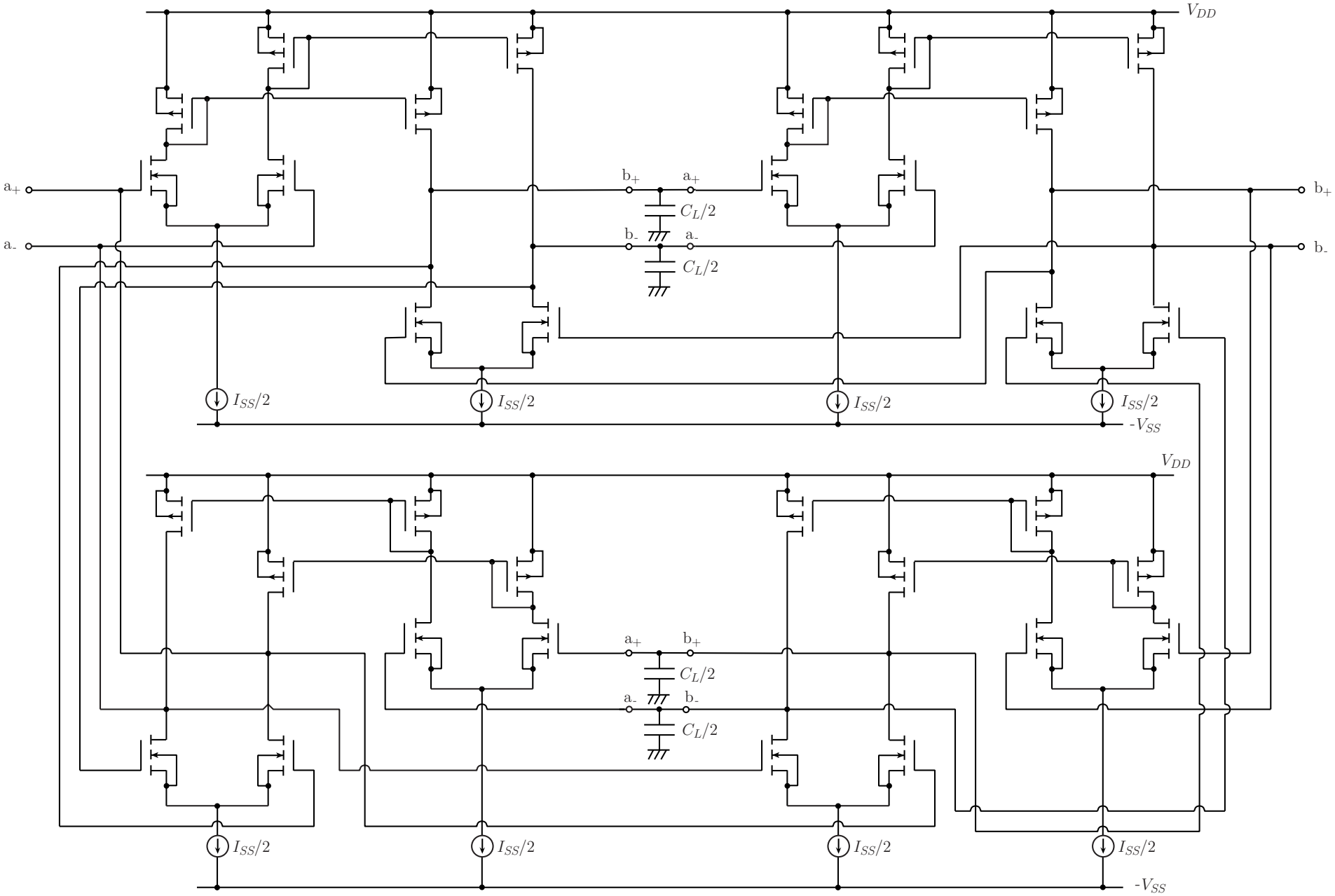


Inductor Dividing Technique




a+
a-
Balanced-Type
2-Port Gyrator
b+
b-
a+
a-
C_L
C_L
Balanced-Type
2-Port Gyrator
b+
b-
Balanced-Type
2-Port Gyrator
(Half Size)
$C_L/2$
$C_L/2$
$C_L/2$
$C_L/2$

Proposed Balanced-Type Inductor



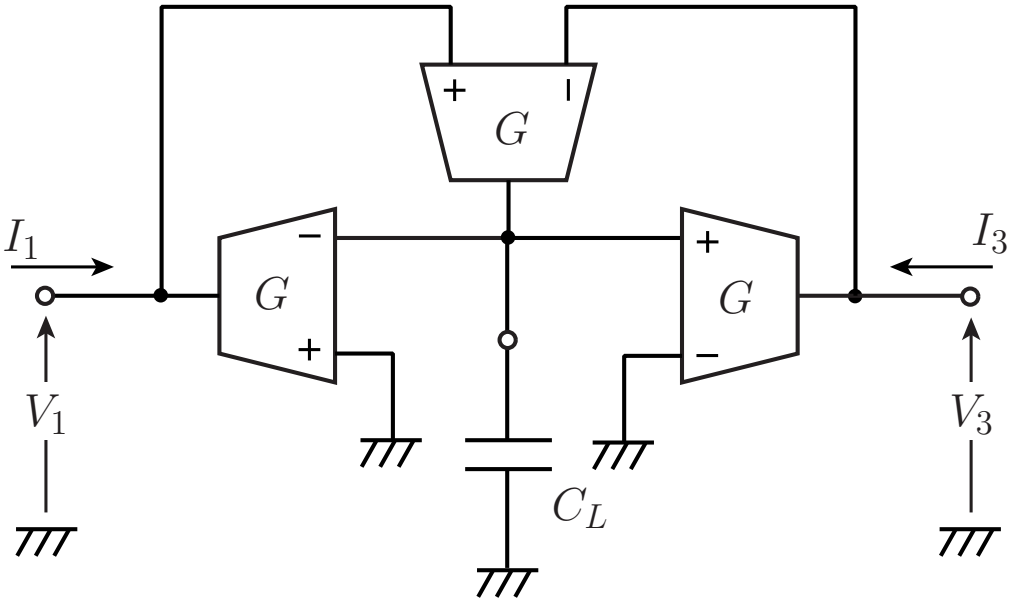
Proposed Inductor Simulation

Specifications

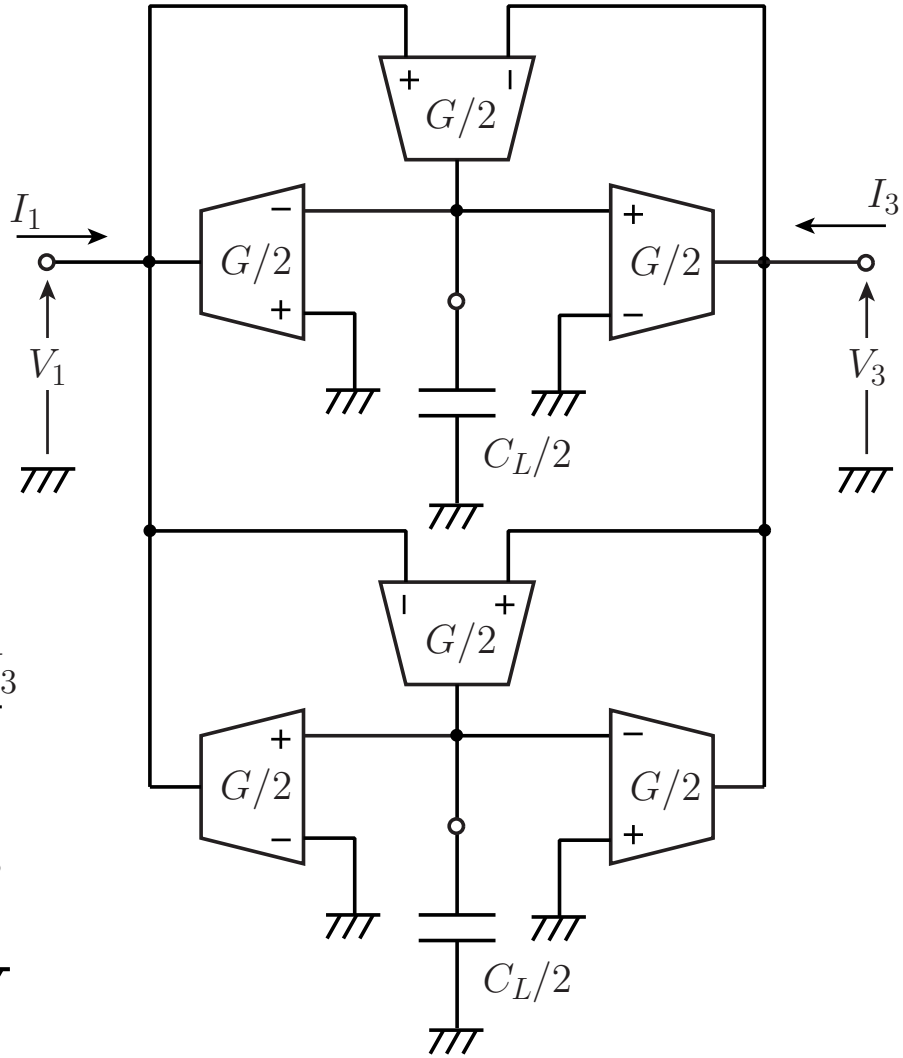
- 0.18-μm CMOS Process
- Supply Voltage: 1.8-V Single Supply
- Inductance: 28μH

Evaluation Items

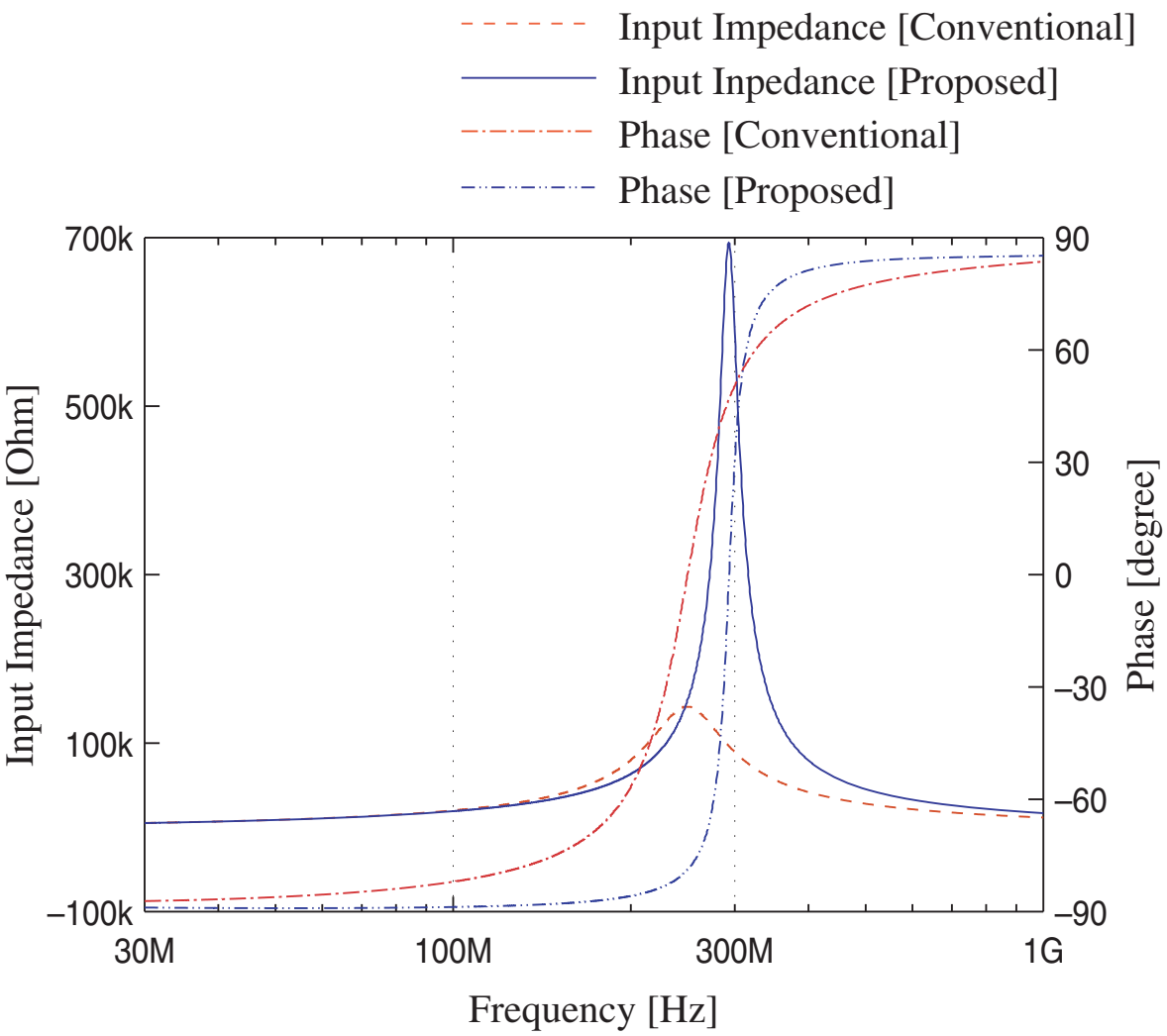
- Power Consumption (Chip Area)
- Frequency Characteristics
- Parasitics



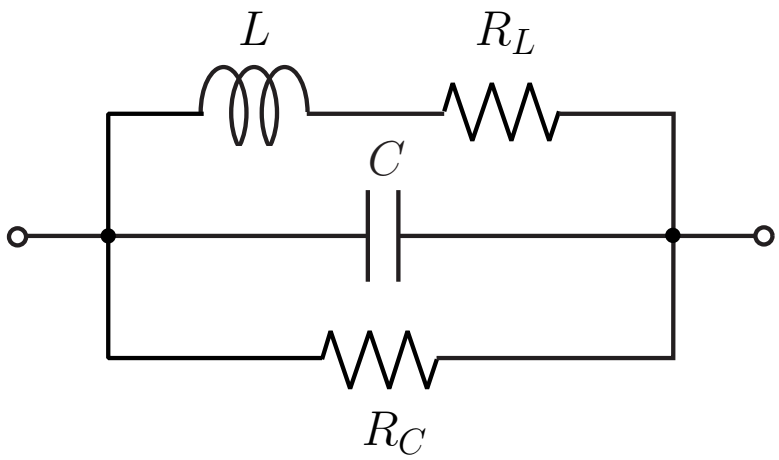
630μW



430μW



Small Circuit Area → Small Parasitics



Active Inductor Equivalent Circuit

Circuit	$L[\mu\mathrm{H}]$	$R_L[\Omega]$	$C[\mathrm{fF}]$	$R_C[\mathrm{k}\Omega]$
Conventional (left)	28	77	15.7	102
Conventional (right)	28	76	14.5	145
Proposed	28	76	10.5	730
Proposed (Balanced)	28	77	13.0	730

Conclusions

- OTA Sharing Technique
- Inductor Dividing Technique
- Current Source Cancelling Technique

Reference:
``Low Power Active Inductor Using Symmetrical Structure,”
T. Sato, S. Takagi, N. Fujii, IEEJ Trans. EIS, Vol.129, No.8,
pp. 1534-1540, 2009 (in Japanese).

Future Works

- Use of finer process for G-Hz range applications
- Noise analysis
- Others