

Communications and Computer Engineering II (ICT.A413)

(情報通信工学統合論 II)

Day/Period(Room No.): 3Q Mon 1-2 (S221), Thu 1-2 (S221)

2016.9.26

Course schedule 2016:

Day/Lecturer	Title/Abstract
1: Sep.26(Mon) Takagi Shigetaka	Analog Integrated Circuits 1: Fundamentals Properties of basic elements for analog integrated circuits and its synthesis are introduced.
2: Sep.29(Thu) Takagi Shigetaka	Analog Integrated Circuits 2: Synthesis Active inductor designs based on a simple circuit given in the first lecture from the viewpoints of power consumption and area efficiency are introduced.
3: Oct.3(Mon) Takahashi Atsushi	Digital Integrated Circuits 1: Fundamentals The basic components of digital integrated circuits and its behavior are introduced.
4: Oct.6(Thu) Takahashi Atsushi	Digital Integrated Circuits 2: Synthesis The basic of discrete structure and algorithm as well as advances of VLSI and its design methodologies are introduced.
5: Oct.13(Thu) Nakahara Hiroki	Logic Functions and FPGA 1: Fundamentals Complexity and functional decomposition of logic functions, and its application for the memory based circuit on the Field Programmable Gate Array (FPGA) are introduced.
6: Oct.17(Mon) Nakahara Hiroki	Logic Functions and FPGA 2: Synthesis Design method for FPGA including a high-level synthesis design are introduced.
7: Oct.20(Thu) Issiki Tsuyoshi	Microprocessor 1 : Instruction-Set Architecture Instruction-set architecture including assembly language and binary machine code and the basic functional behavior of microprocessor is explained.
8: Oct.24(Mon) Issiki Tsuyoshi	Microprocessor 2 : Processor Micro-architecture Basic processor micro-architecture including register-file, memories, caches, instruction decoder and ALU are explained.
9: Oct.27(Thu) Sugino Nobuhiko	Compiler 1: Fundamentals Procedures of a compiler (Front-End, Intermediate Codes, and Back-End) are introduced.
10: Oct.31(Mon) Sugino Nobuhiko	Compiler 2: Code Optimization Techniques Various code optimization techniques and programming techniques for higher performance are given. And, then, code optimization techniques for embedded processors are discussed.
11: Nov.3(Thu) Nakahara Hiroki	Computer System 1: Deep Neural Network Trend for the deep neural network (DNN) and applications using DNN are introduced.
12: Nov.7(Mon) Hara Yuko	Embedded Systems 1: Fundamentals and RTOS Overview of embedded systems and fundamental technologies of embedded software, especially about real-time operating systems (RTOS) are introduced.
13: Nov.10(Thu) Hara Yuko	Embedded Systems 2: Embedded Hardware Synthesis High-level design methodologies of embedded hardware, such as high-level synthesis, are introduced.
14: Nov.14(Mon) Nakamoto Takamichi	Digital Integrated Circuit Design using HDL Design of digital integrated circuit using hardware description language (HDL) are explained.
15: Nov.17(Thu) Nakamoto Takamichi	Computer System 2: Sensing System Principle of a sensor based on its frequency change and its measurement circuit using FPGA are explained.

Reference books, course materials, etc.:

Handouts will be distributed at the beginning of class when necessary

Assessment criteria and methods:

Learning achievement is evaluated by the quality of the written reports, exercise problems, and etc.

Related courses: ICT.A402 : Communications and Computer Engineering I

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Contact each lecturer directly for each class and report.

Office hours: Contact by e-mail in advance to schedule an appointment