## Problem 4.1

Consider the NAND2-tree in Fig.1.
A) Using the cell library shown in Fig. 2 (next page : note that NOR2 gate is added), give an area optimal technology mapping. Also show the intermediate covering results on the subtrees rooted at each node.

- For simplicity, you don't have to consider the "powered" cells, since area optimal covering will always use the smaller "unpowered" cells only.
B) For the same problem, give a delay optimal technology mapping with the same cell library.
- Assume that a load of 2 to 6 is connected to the output of the root (node 11) and derive the mapping solutions for each of the load value.
- For each different mapping solutions derived, compute the slack times at each mapped cell, and apply area recovery if possible.


Fig. 1 Target NAND2-tree

| symbol | cell name | area | gate <br> load | switching delay | output transition coef |
| :---: | :---: | :---: | :---: | :---: | :---: |
| - | INV | 2 | 3 | 12 | 4 |
|  | INVP | 3 | 6 | 12 | 2 |
|  | NAND2 | 3 | 3 | 25 | 6 |
|  | NAND2P | 5 | 6 | 25 | 3 |
|  | NAND3 | 4 | 2 | 40 | 8 |
|  | NAND3P | 7 | 4 | 40 | 4 |
|  | NAND4 | 5 | 2 | 60 | 8 |
|  | NAND4P | 9 | 4 | 60 | 4 |
|  | AOI21 | 4 | 3 | 60 | 8 |
|  | AOI21P | 7 | 6 | 60 | 4 |
|  | NOR2 | 3 | 3 | 25 | 6 |
|  | NOR2P | 5 | 6 | 25 | 3 |

Fig. 2 : Cell library. Assume that all input pins have the same load and switch delay for each cell in this library

## Problem 4.2

Consider the fan-out network in Fig.3.

- An inverter with cell switching delay $S_{r}=12$ and output transition coefficient $T_{r}=4$ is driving the 8 loads whose required times are indicated by $R_{i}$ and input gate loads indicated by $L_{i}(i=0,1, \ldots, 7)$.
A) Construct a fan-out tree by Two-Level Tree algorithm using the buffer cell $b_{1}$ shown in Fig. 4 .
B) Construct a fan-out tree by Combinational Merging algorithm using the buffer cell $b_{1}$ and $b_{2}$ shown in Fig.4.


Fig. 3 Fan-out network


Fig. 4 Buffer cell $b_{1}$ and cell $b_{2}$

