平成26年度前期東京工業大学学部講義

電子デバイス

Electron Devices

資料（7）　Handout

Handout
5／19
に講義時に配付したもの。
修正が入ってないので、修正版を参考にすること。

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Green ICE Tokyo Tech Information Communication Energy
Semiconductor Solution Research

TOKYO TECH Pursuing Excellence

講義日程・内容（平成26年度）

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1. 4月 7日（月） pn接合の復習
2. 4月14日（月） 半導体デバイスと集積回路
3. 4月21日（月） ﾊﾞｲﾎﾟｰﾗﾄﾗﾝｼﾞｽﾀ（Ⅰ）：構造と理想I-V特性
4. 4月28日（月） ﾊﾞｲﾎﾟｰﾗﾄﾗﾝｼﾞｽﾀ（Ⅱ）：等価回路モデル
5. 5月 7日（水） ﾊﾞｲﾎﾟｰﾗﾄﾗﾝｼﾞｽﾀ（Ⅲ）：デバイス設計
6. 5月12日（月） ﾊﾞｲﾎﾟｰﾗﾄﾗﾝｼﾞｽﾀ（Ⅳ）：動作速度
7. 5月19日（月） MOSダイオード
8. 5月26日（月） 中間試験
9. 6月 2日（月） MOSトランジスタ（Ⅰ）：構造と基本I-V特性
10. 6月 9日（月） MOSトランジスタ（Ⅱ）：Scaling、SCE
11. 6月16日（月） MOSトランジスタ（Ⅲ）：動作速度
12. 6月23日（月） MOSトランジスタ（Ⅳ）：CMOS基本回路
13. 6月30日（月） MOSトランジスタ（Ⅴ）：作製プロセス
14. 7月 7日（月） メモリデバイス，パワーデバイス
15. 7月14日（月） 期末試験

5月26日（月）中間試験：試験範囲は4/7～5/12まで。 前半：益、後半：大見

Today's purpose

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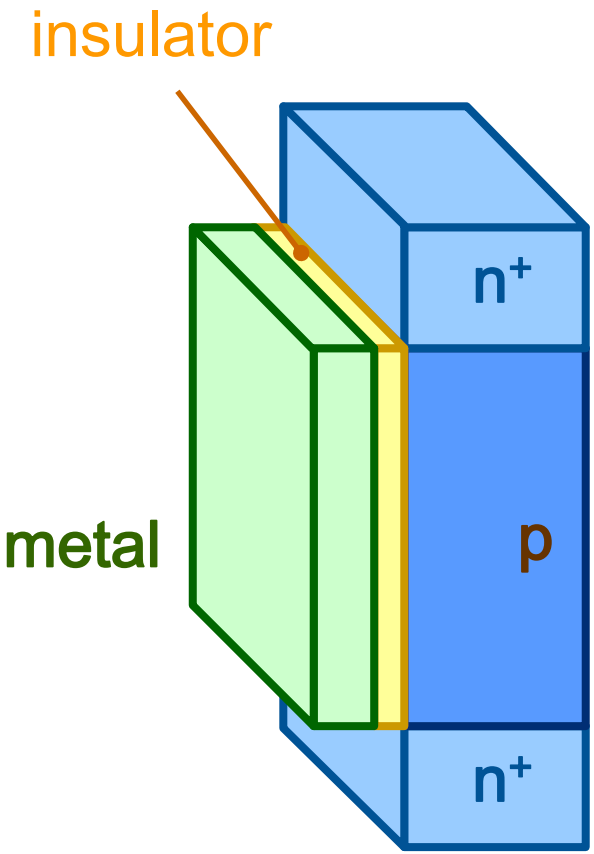
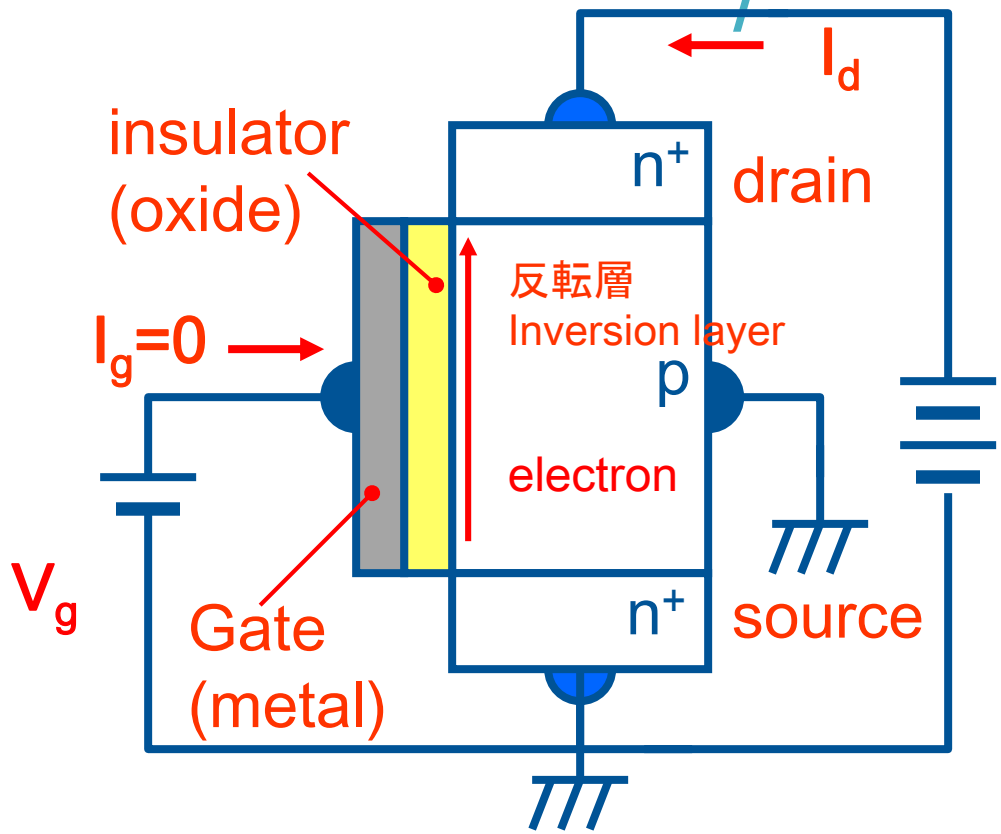
- MOS diode structure
- What is the ideal MOS structure?
- Band diagram with various bias condition
- To understand accumulation（蓄積）, depletion（空乏）, inversion（反転）, and strong inversion（強反転）in band diagram.
- Derivation of threshold voltage（しきい値電圧、閾値電圧）that is required for the strong inversion

MOSFET





3-terminal device in which the current from source to drain is controlled by gate voltage V_g

$I_d = g_m V_g$, g_m:mutual conductance（相互ｺﾝﾀﾞｸﾀﾝｽ）

MOSFETの構造

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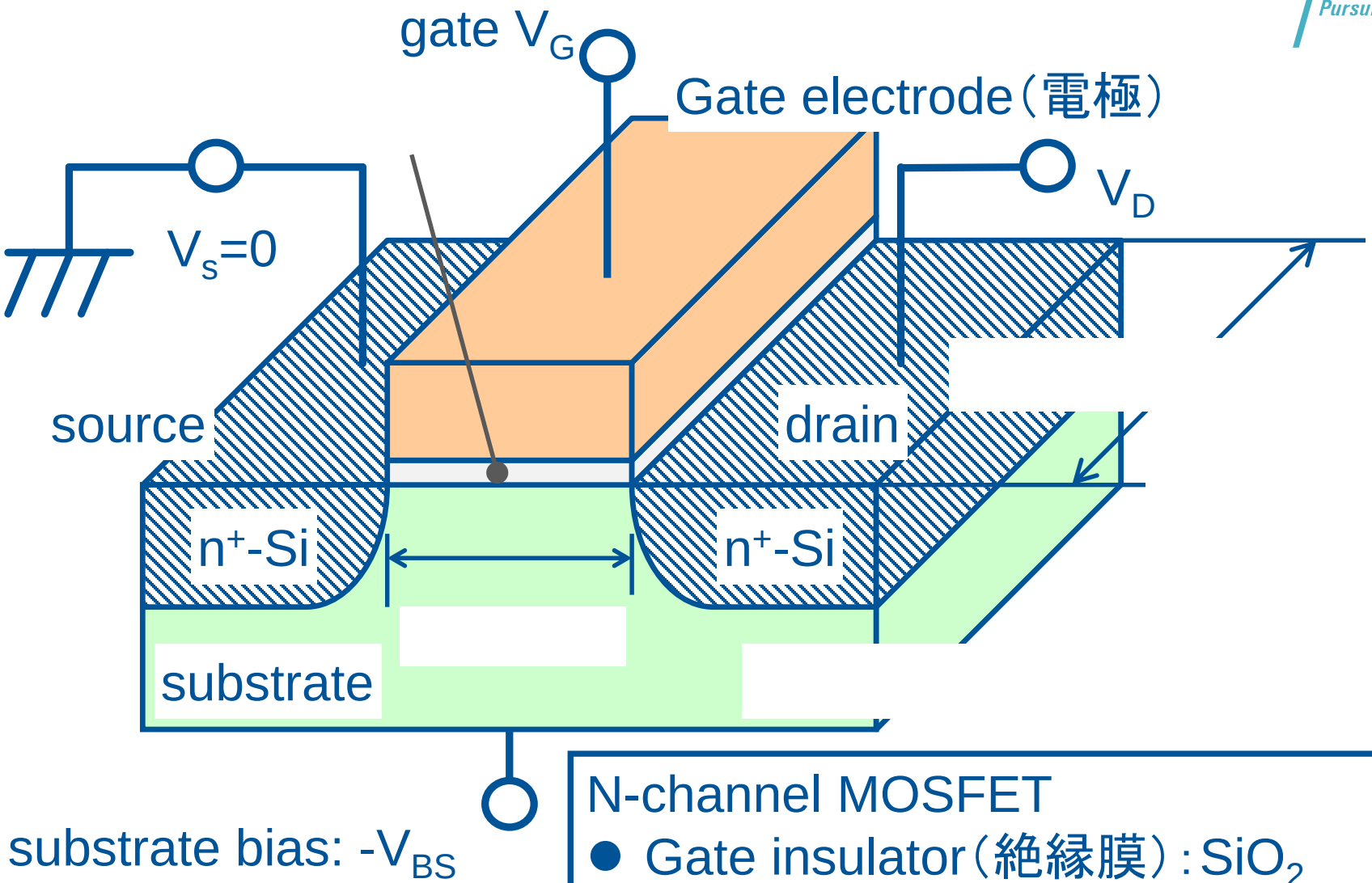

N-channel MOSFET

- Gate insulator（絶縁膜）: SiO_2
- Gate electrode : formerly Al → poly-Si→metal

Parameters for MOSFET

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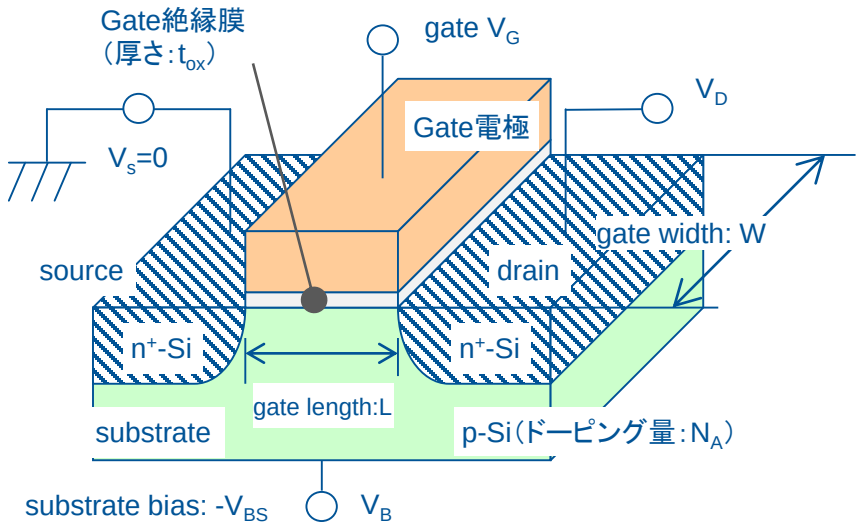
English



- Structural quantities

- Physical parameters
  - Relative permittivity（Si）: ε_{Si}
  - relative permittivity（SiO_2）: ε_{ox}
  - Electron affinity（Si）: χ_{Si}
  - Band gap（Si）: E_g
  - mobility: μ

- Parameters for circuit
  - Drain voltage $V_{DS} = V_D - V_S$
  - Gate voltage $V_{GS} = V_G - V_S$
  - Substrate bias（back bias）
    $-V_{BS} = -V_B + V_S$

- t_{ox}， N_A: Parameters which determined during process development
- L and W:

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Parameters for MOSFET

presentation
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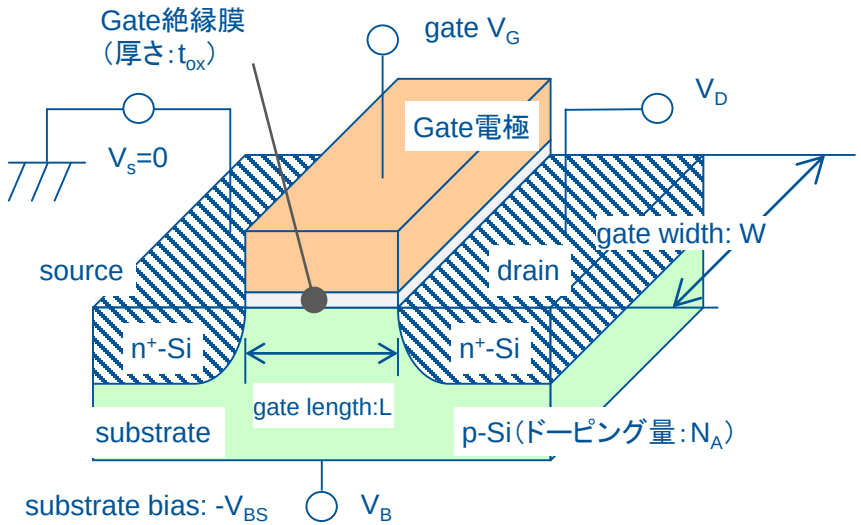
Japanese



- 構造に関わる量
  - ゲート長: L [m]
  - ゲート幅: W [m]
  - 絶縁膜厚さ: t_{ox} [m]
  - 基板濃度: N_A [m^{-3}]
- 物性量
  - 比誘電率（Si）: ε_{Si}
  - 比誘電率（SiO_2）: ε_{ox}
  - 電子親和力（Si）: χ_{Si}
  - 禁制帯幅（Si）: Eg
  - 移動度: μ

- 回路関係
  - ドレイン電圧 $V_{DS} = V_D - V_S$
  - ゲート電圧 $V_{GS} = V_G - V_S$
  - 基板電圧（back bias）
    $-V_{BS} = -V_B + V_S$

- プロセス構築時に決まる量: t_{ox}, N_A
- 回路設計者が扱える量: L and W

Metal-insulator-semiconductor band diagram (1)

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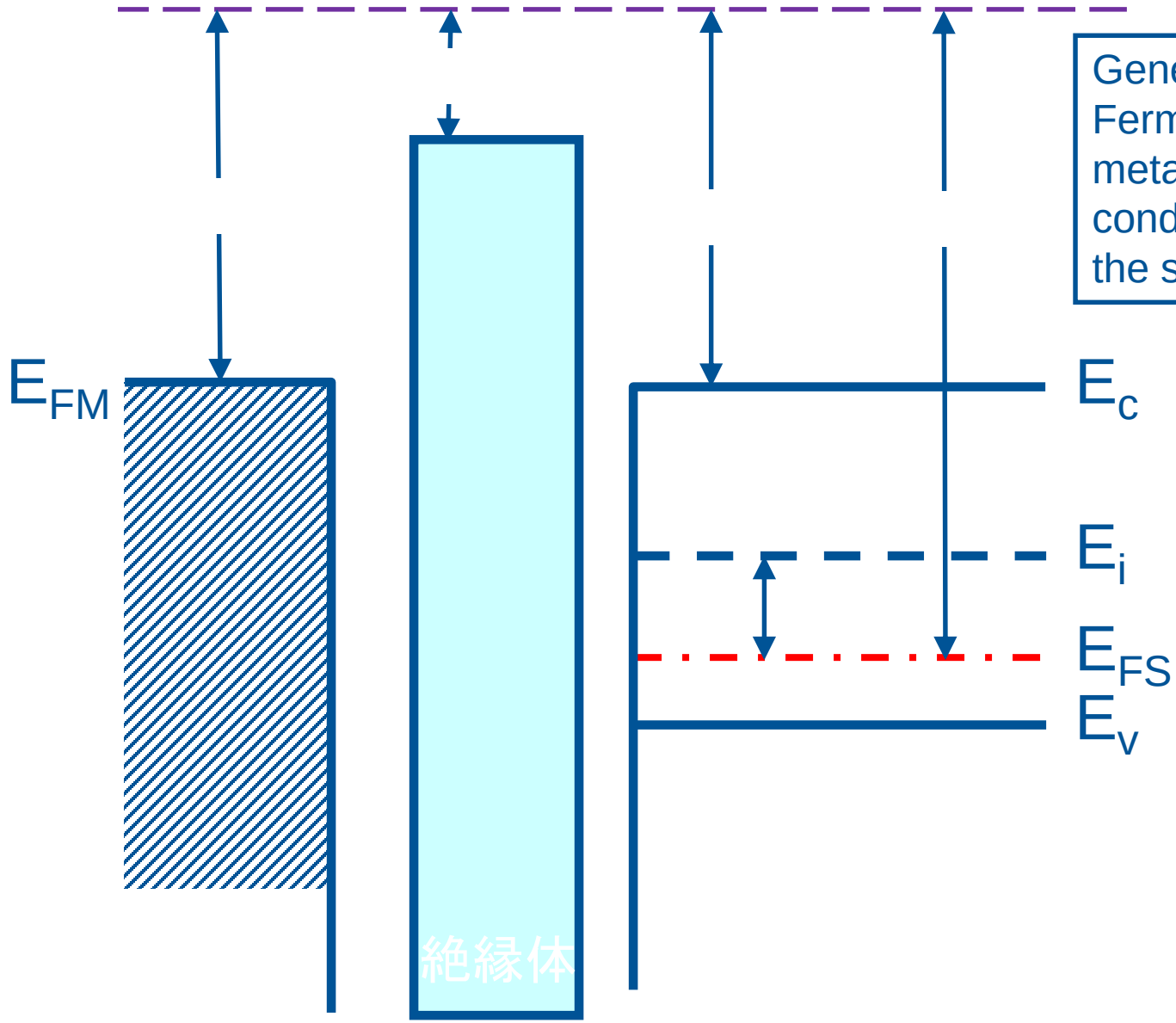
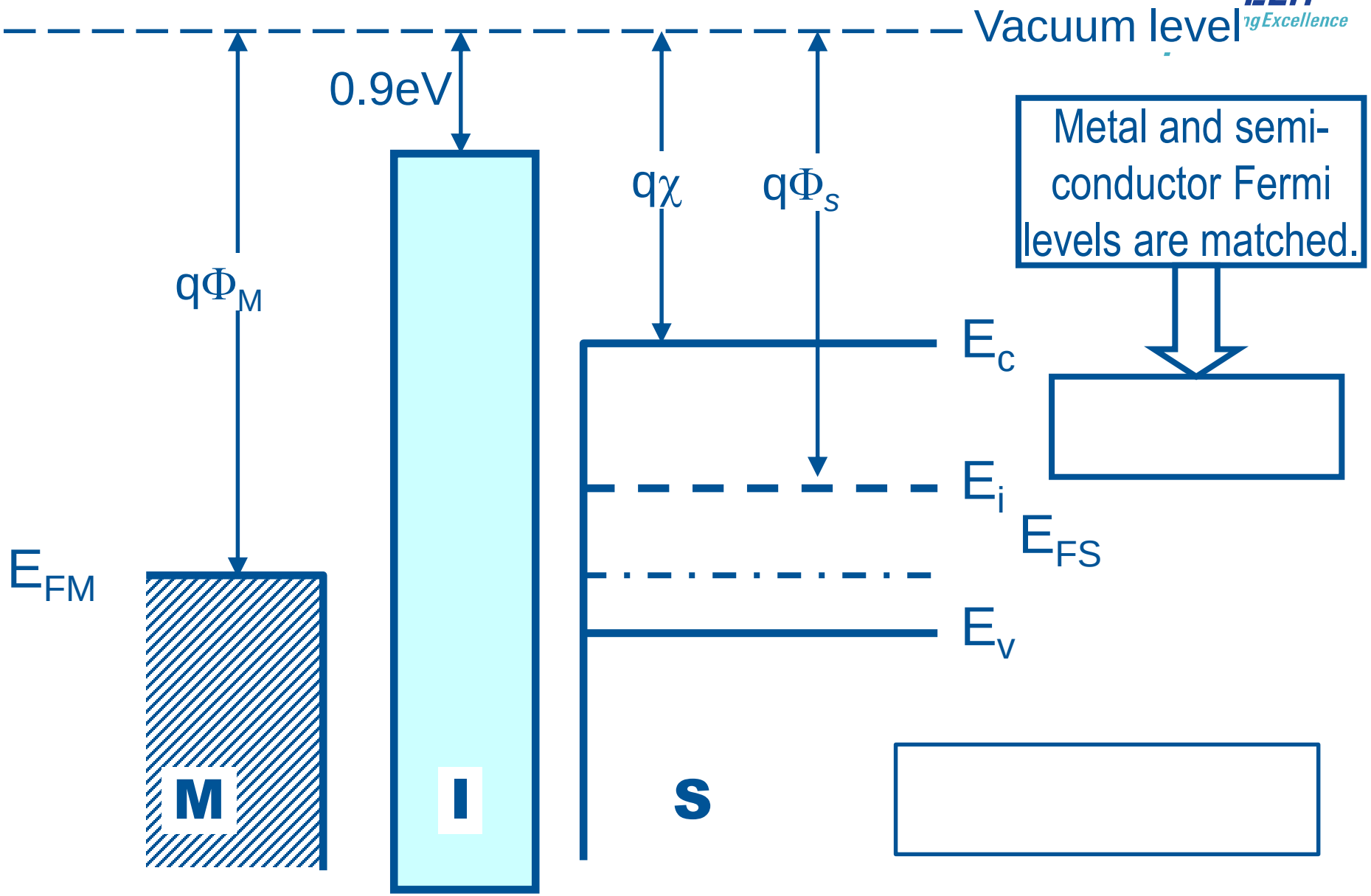


General case: Fermi levels of metal and semi-conductor are not the same.

Metal-insulator-semiconductor band diagram (2)

handout



Ideal MIS diode: definition (1)

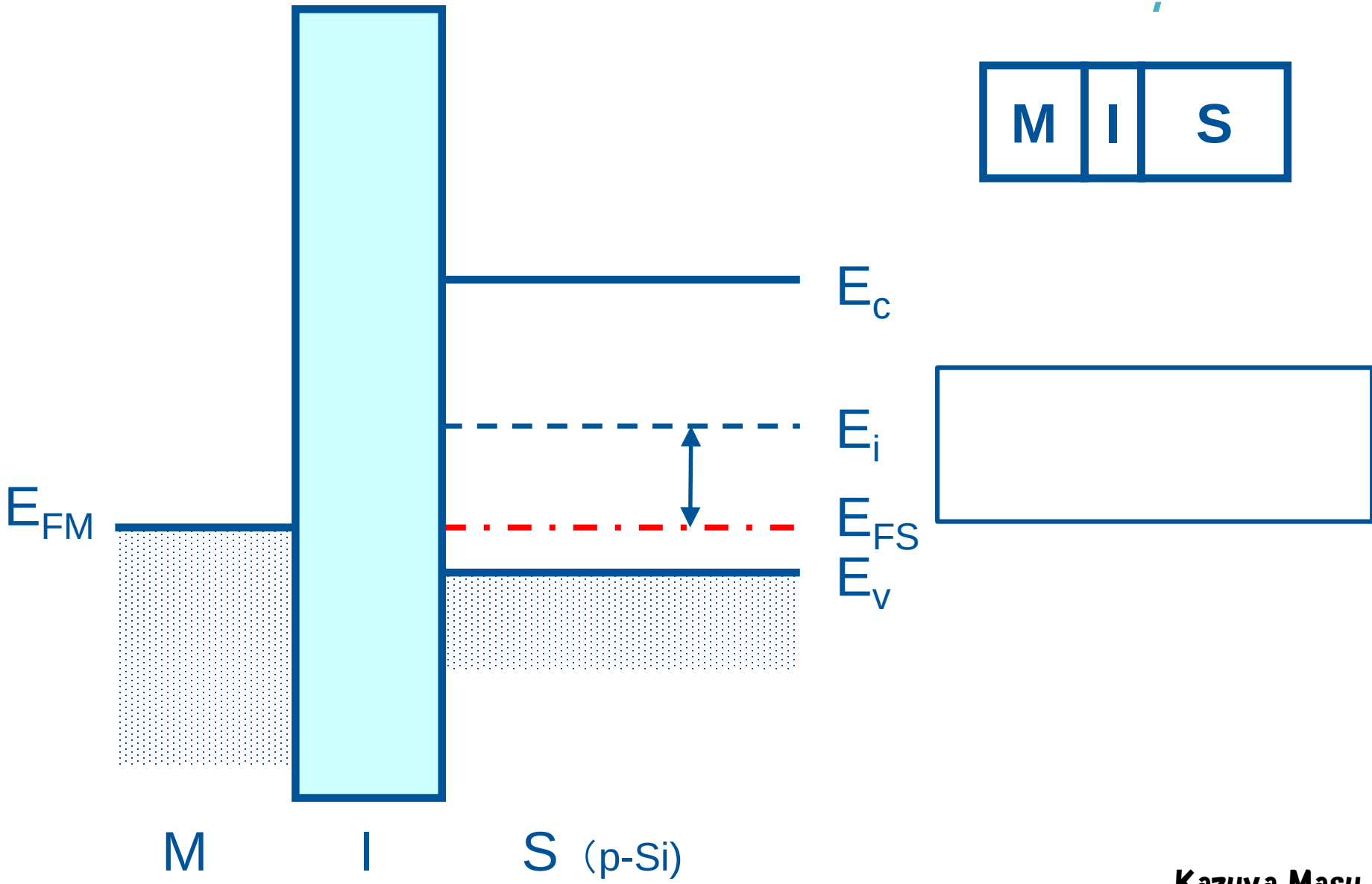
1.

2.

Ideal MIS diode: definition (2)

3.

Ideal MIS diode (1)



Ideal MIS diode (2)

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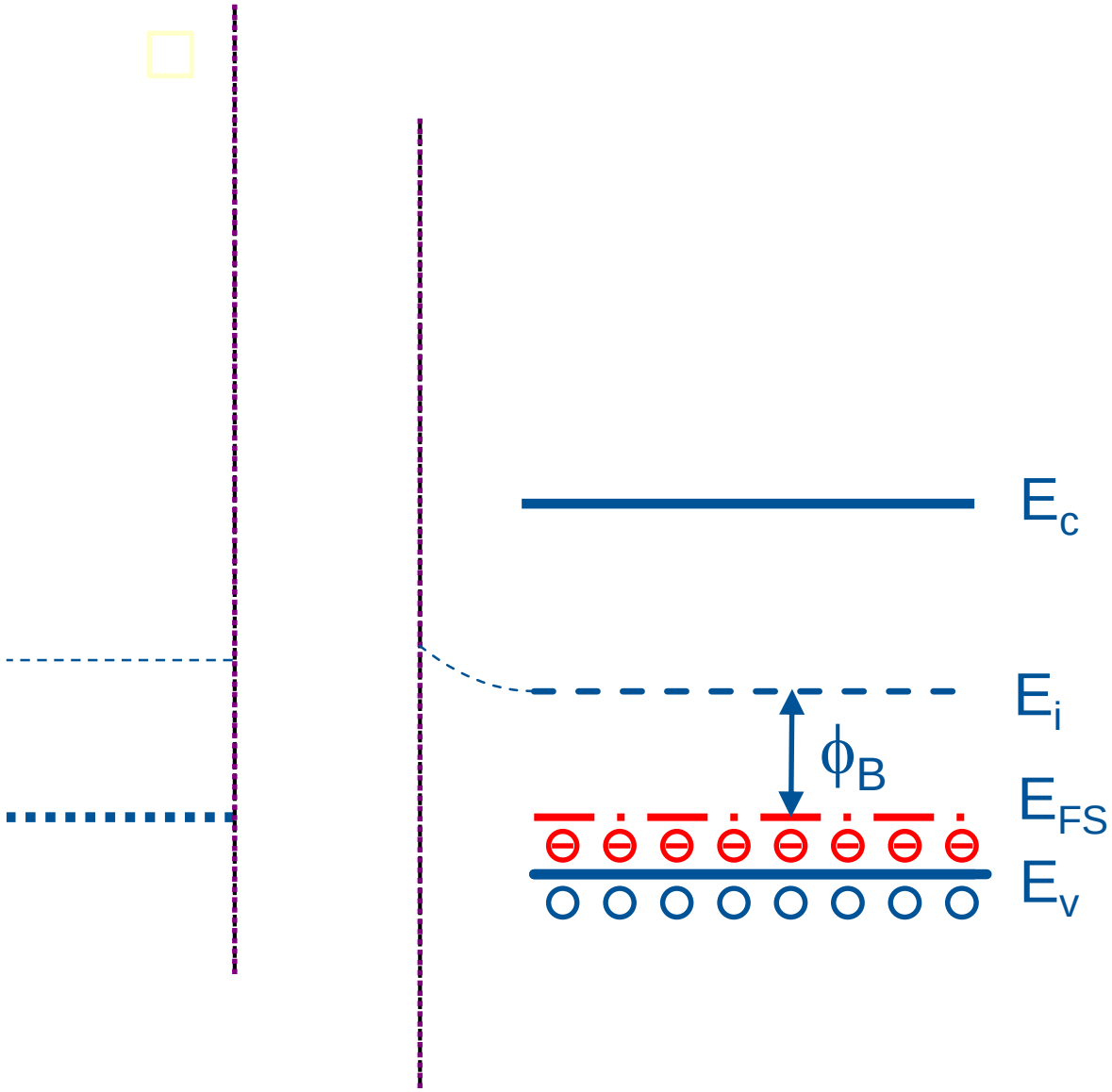
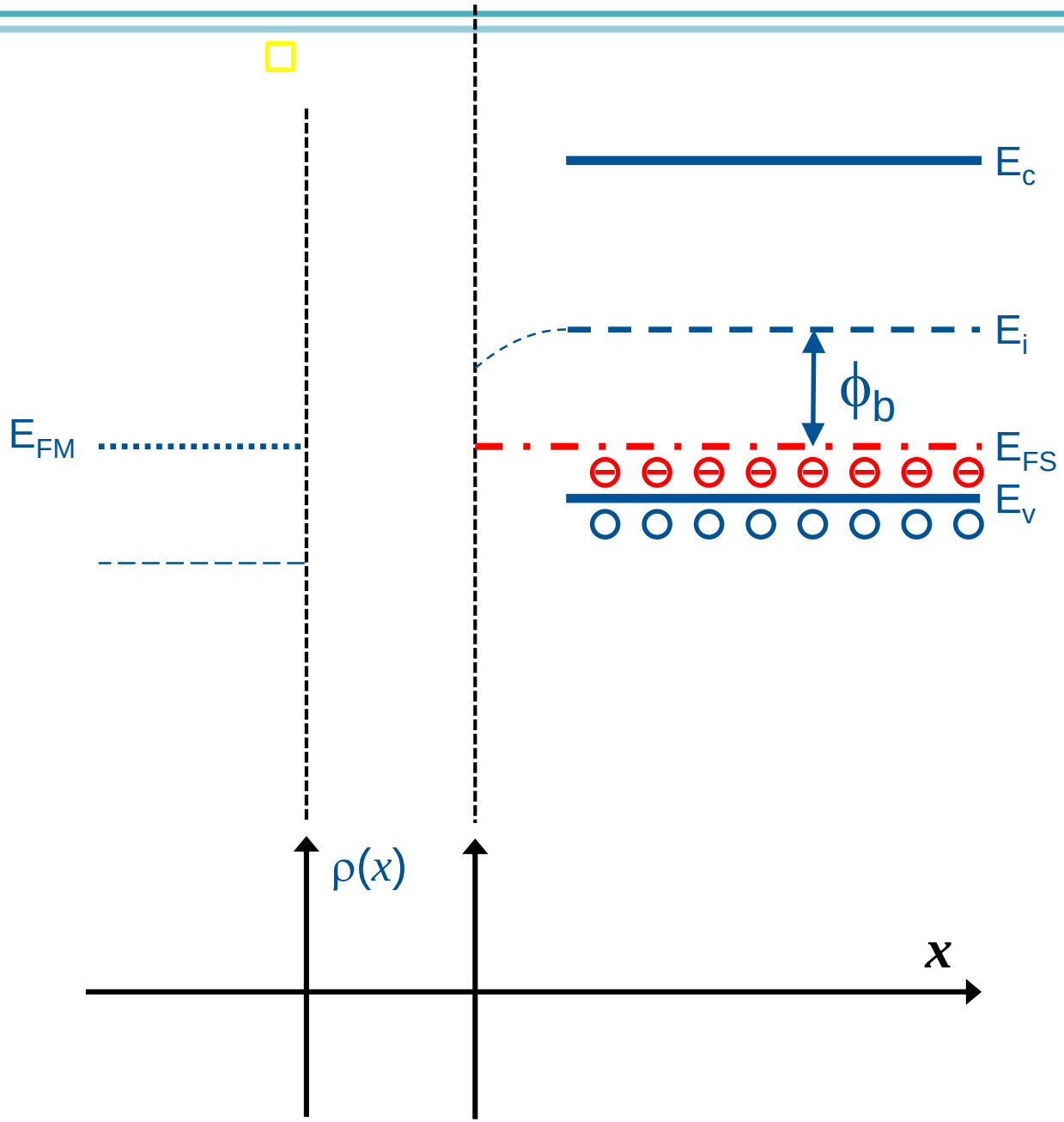
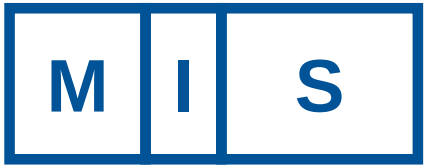
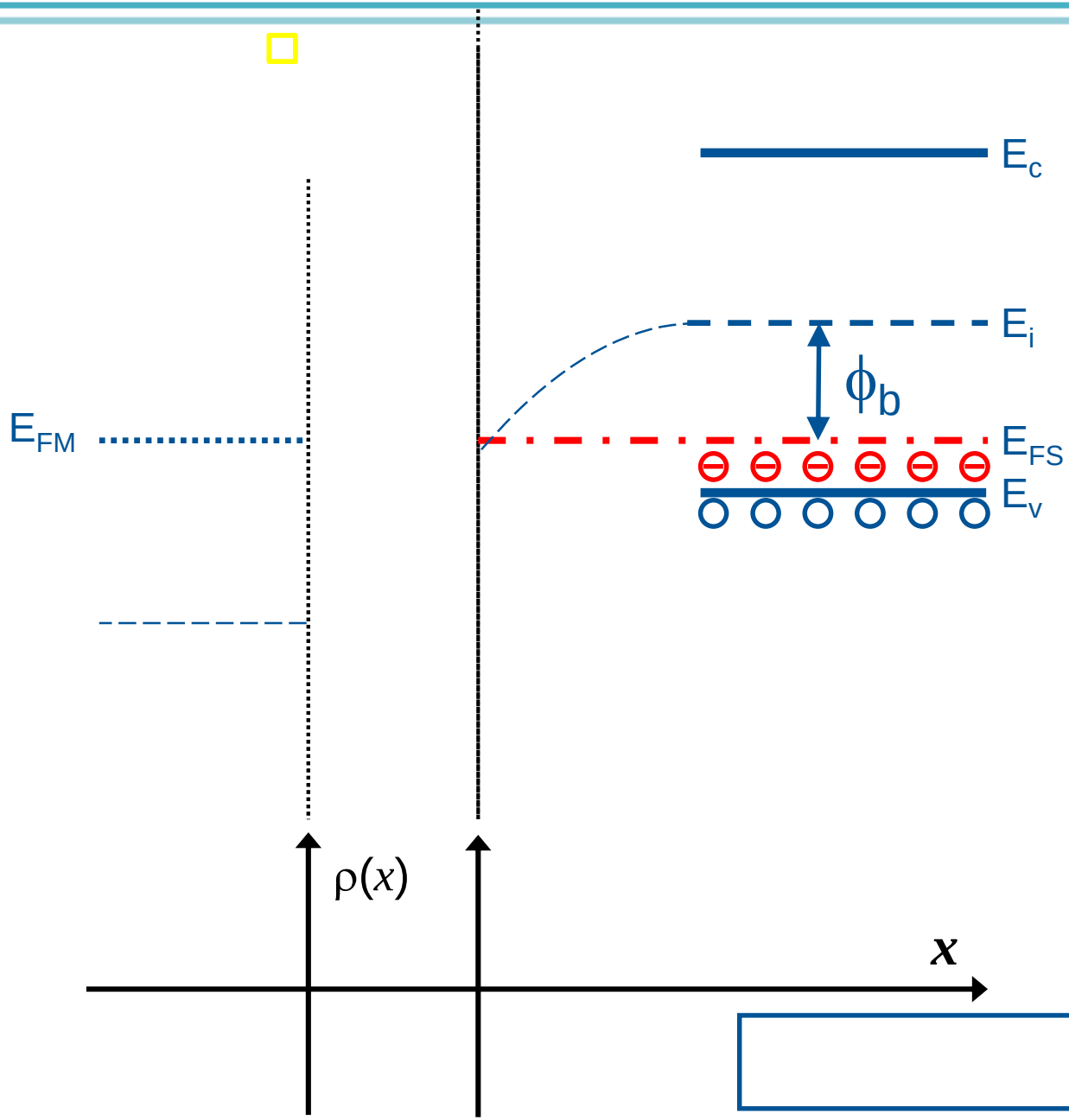


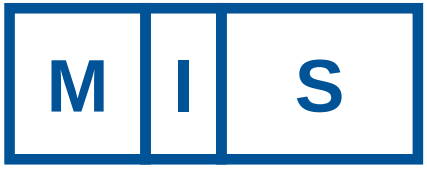
Ideal MIS diode (3)





Ideal MIS diode (4)





Ideal MIS diode (5)（強反転　strong inversion）

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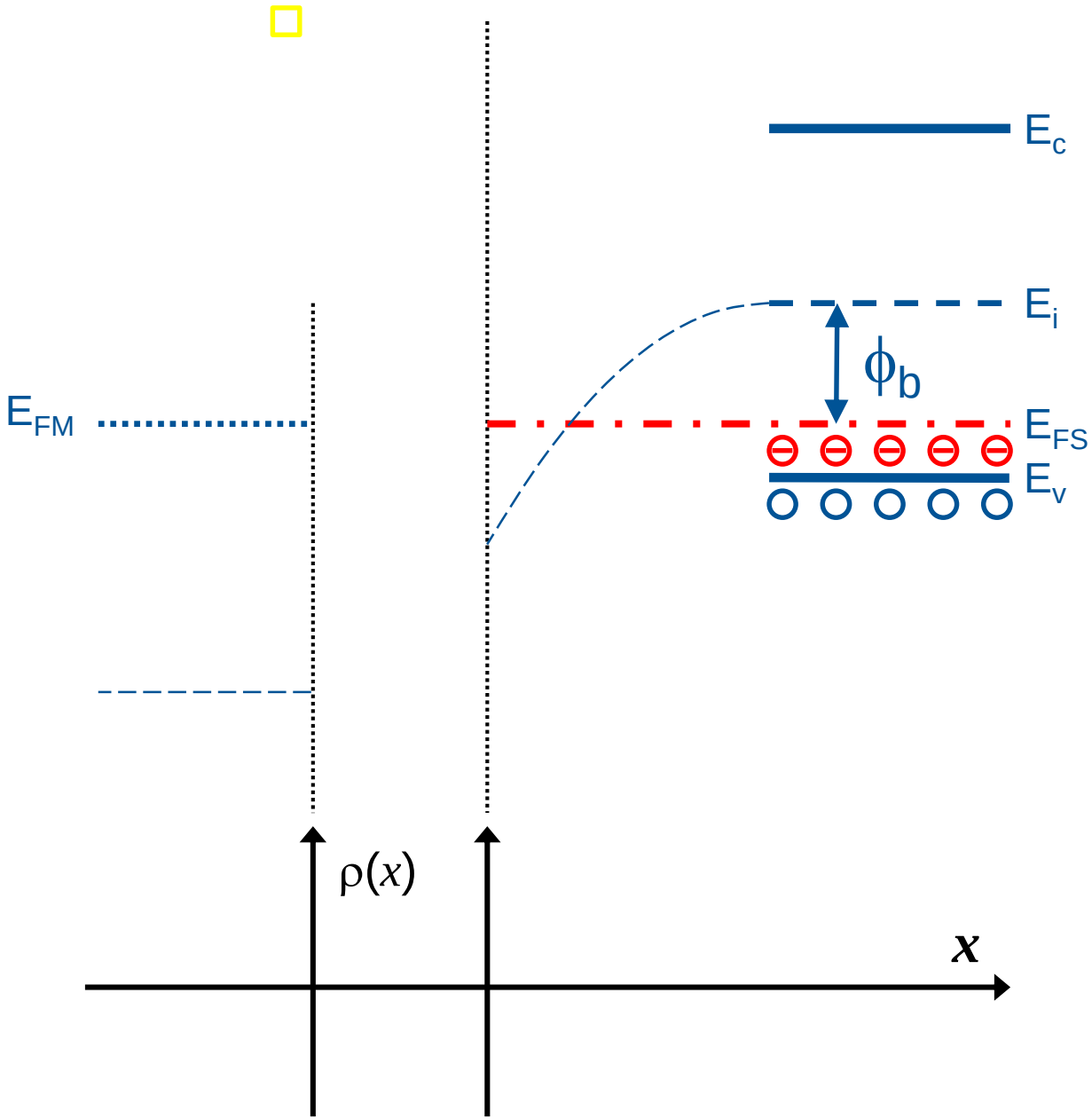
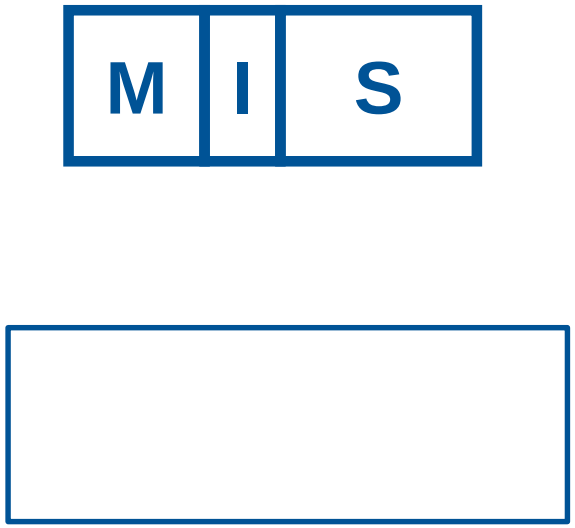




Summary: Ideal MIS diode in strong inversion (1)

1. Strong inversion（　　）:
2. How does the band diagram change with a larger gate voltage than that for $\varphi_s = 2\phi_b$? （

   a. The energy band does not bend further.

   b. The electron in the inversion layer is increased. The small band bending causes the exponential increase of electron.

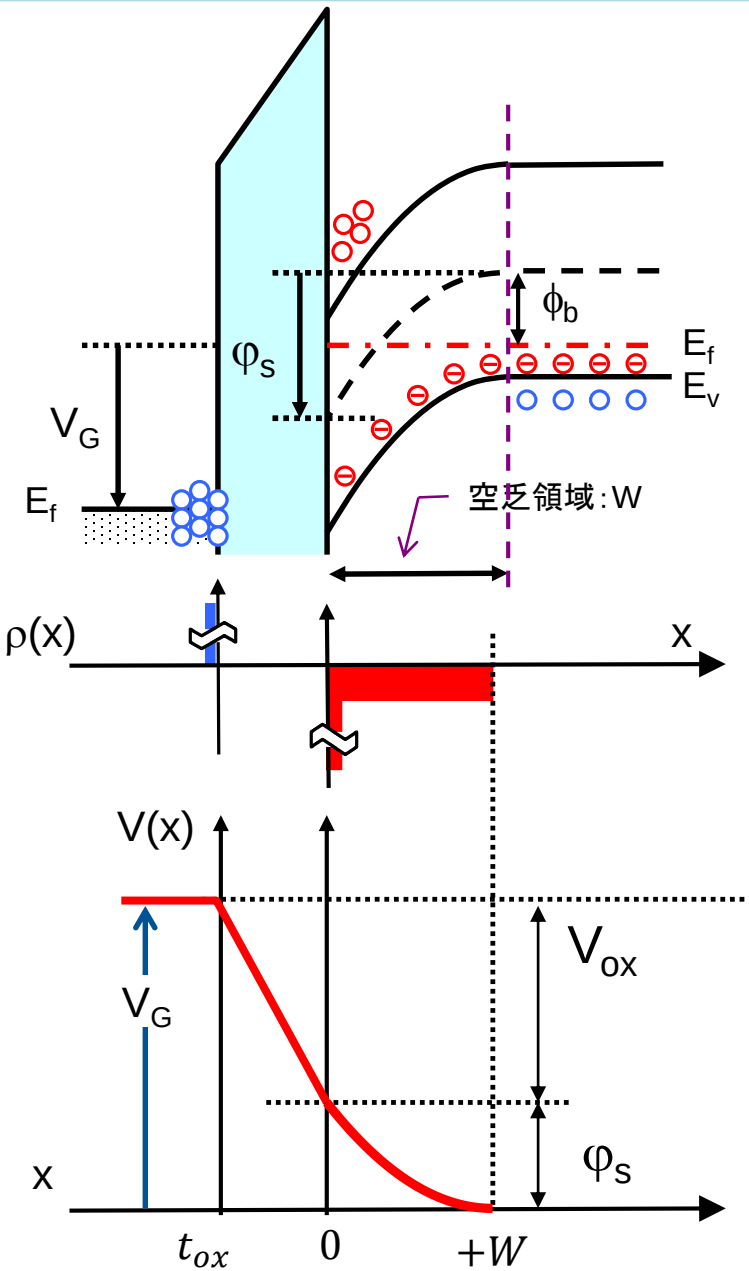
Ideal MIS diode in strong inversion (2)

c. The width of depletion layer is not increased; The width becomes the maximum width W_{max}.

d. The electric field line from the metal surface is terminated at the electrons in the inversion layer when the applied gate voltage is larger than that required for the strong inversion.

3. In MOSFET, the electron in the inversion layer is origin of drain current.

Surface potential φ_s in the strong inversion



- Assumption: The charge that exist in the depletion region is only the ionized acceptor atom and its density is constant. (depletion-layer approximation) （空乏近似：空乏層にはイオン化したアクセプタのみ存在）
- Poisson's equation

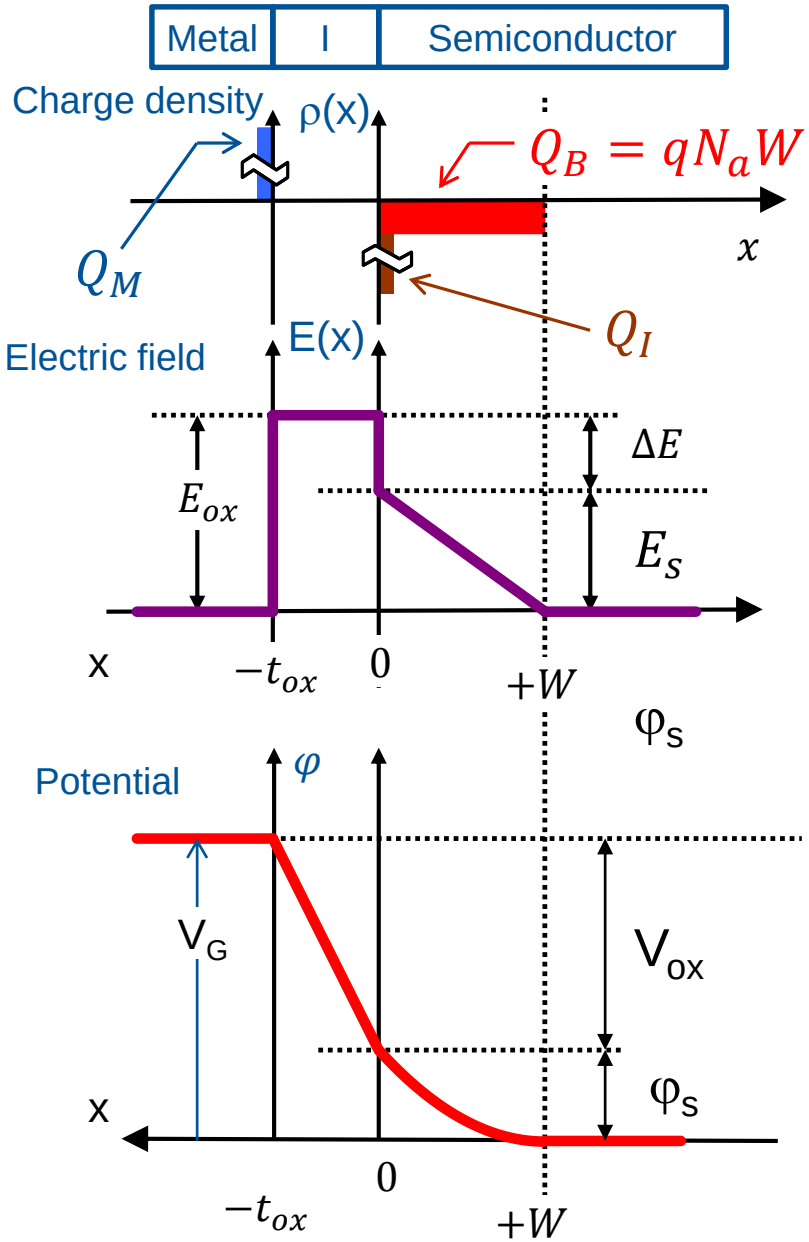
$$\frac{d^2\varphi(x)}{d\,x^2} = +\frac{qN_a}{\varepsilon} \cdots (1)$$

$$for\ 0 \le x \le \mathrm{W}$$

- Boundary conditions

$$\varphi(+W) = 0, \varphi(0) = \varphi_s$$

Surface potential φ_s in the strong inversion



$$\varphi(x) = \frac{qN_a}{2\varepsilon}(x - W)^2 \cdots (2)$$

$$E_s = -\frac{d\varphi(x)}{dx} = \frac{qN_a}{\varepsilon}(W - x) \cdots (3)$$

- In the strong inversion, the depletion layer width is W_m. The surface potential of the strong inversion φ_s^{inv} is given by $\varphi(0)$.

- On other hand, $\varphi_s = 2\phi_b$

Derivation of threshold voltage

$$\varphi_s^{inv} = 2\phi_b = \frac{qN_a{W_m}^2}{2\varepsilon_o\varepsilon_{Si}} \quad \cdots (5)$$

$$\phi_b = \frac{kT}{q} log_e \frac{N_a}{n_i} \quad \cdots (6)$$

- From eqs.(5) and (6), the maximum depletion layer width is given by

Derivation of threshold voltage

- Charge balance is given by

$$Q_M = Q_I + Q_B \quad \cdots (8)$$

  - Q_M: charge at the metal surface,
  - Q_I: electrons in the inversion layer, and
  - Q_B:ionized acceptor in the depletion region.
- Q_M is given by $Q_M = C_{ox}(V_g - \varphi_s) \quad \cdots (9)$
- $C_{ox} = \varepsilon_{ox}\varepsilon_o / t_{ox}$:the insulator capacitance
- In the depletion approximation, just at the strong inversion, $Q_I = 0, \varphi_s = \varphi_s^{inv} = 2\phi_b, and\ W = W_m$. The gate voltage required for the strong inversion is given by eq.(9)

Derivation of threshold voltage

- From eq.(9)

$$Q_M = \left(V_g - \varphi_s\right) \quad \rightarrow \; V_g = \varphi_s + \frac{Q_M}{C_{ox}}$$

- The threshold voltage that is required for strong inversion is given by

Derivation of threshold voltage

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$$V_{th} = 2\phi_b + \frac{qN_aW_m}{C_{ox}} = 2\phi_b + \frac{\sqrt{2\varepsilon_o\varepsilon_{Si}qN_a(2\phi_b)}}{C_{ox}}$$

The surface potential
（表面ポテンシャル）

The voltage across the insulator
（絶縁膜にかかる電圧）

- The threshold voltage for the ideal MIS diode is determined by

Charges in the inversion layer

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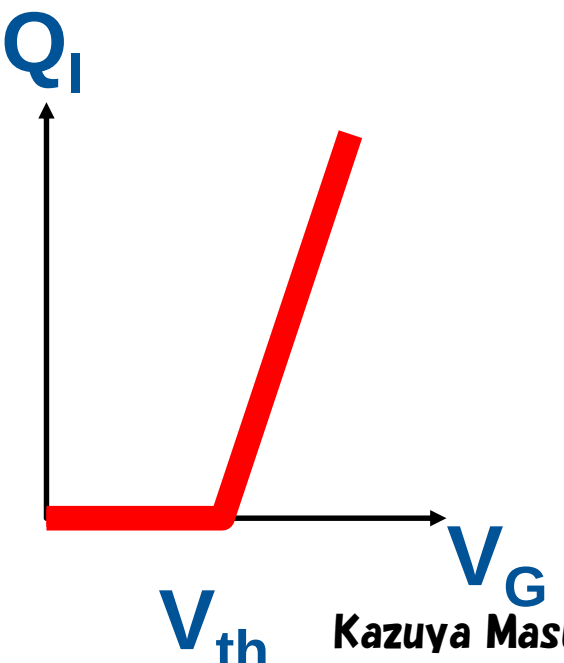
- From eq. (8), the inversion layer charge is given by $Q_I = Q_M - Q_B$

$$Q_I = C_{ox}\left(V_G - \varphi_s^{inv}\right) - qN_aW_m$$
$$= C_{ox}\left\{V_G - \left(\varphi_s^{inv} + \frac{qN_aW_m}{C_{ox}}\right)\right\}$$

$$\therefore \; Q_I = C_{ox}(V_G - V_{th})$$



Kazuya Masu

Charge density as a function of surface potential

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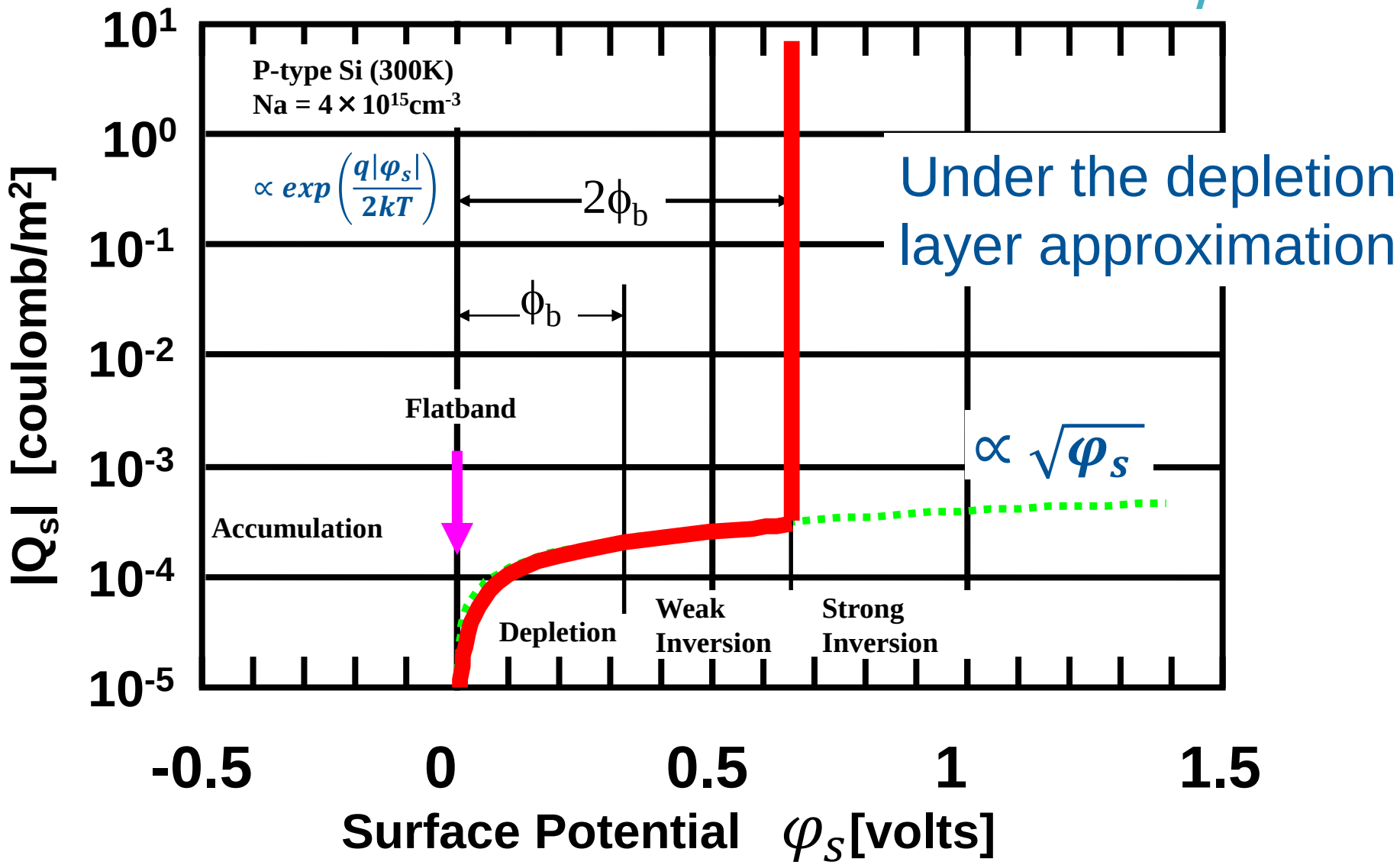
Supplement



Charge density as a function of surface potential

Supplement

- Q_s : the sum of depletion layer charge and inversion layer charge
- Precise analysis gives Q_s as follows:

$$Q_s = -\varepsilon_{Si}\varepsilon_o E_S = \mp \frac{\sqrt{2}\varepsilon_{Si}\varepsilon_o kT}{qL_D} F\left(\beta\varphi_s, \frac{n_{po}}{p_{po}}\right)$$

$$F\left(\beta\varphi, \frac{n_{po}}{p_{po}}\right) = \left[\left(e^{-\beta\varphi} + \beta\varphi - 1\right) + \frac{n_{po}}{p_{po}}\left(e^{+\beta\varphi} - \beta\varphi - 1\right)\right]^{1/2}$$

Charge density as a function of surface potential

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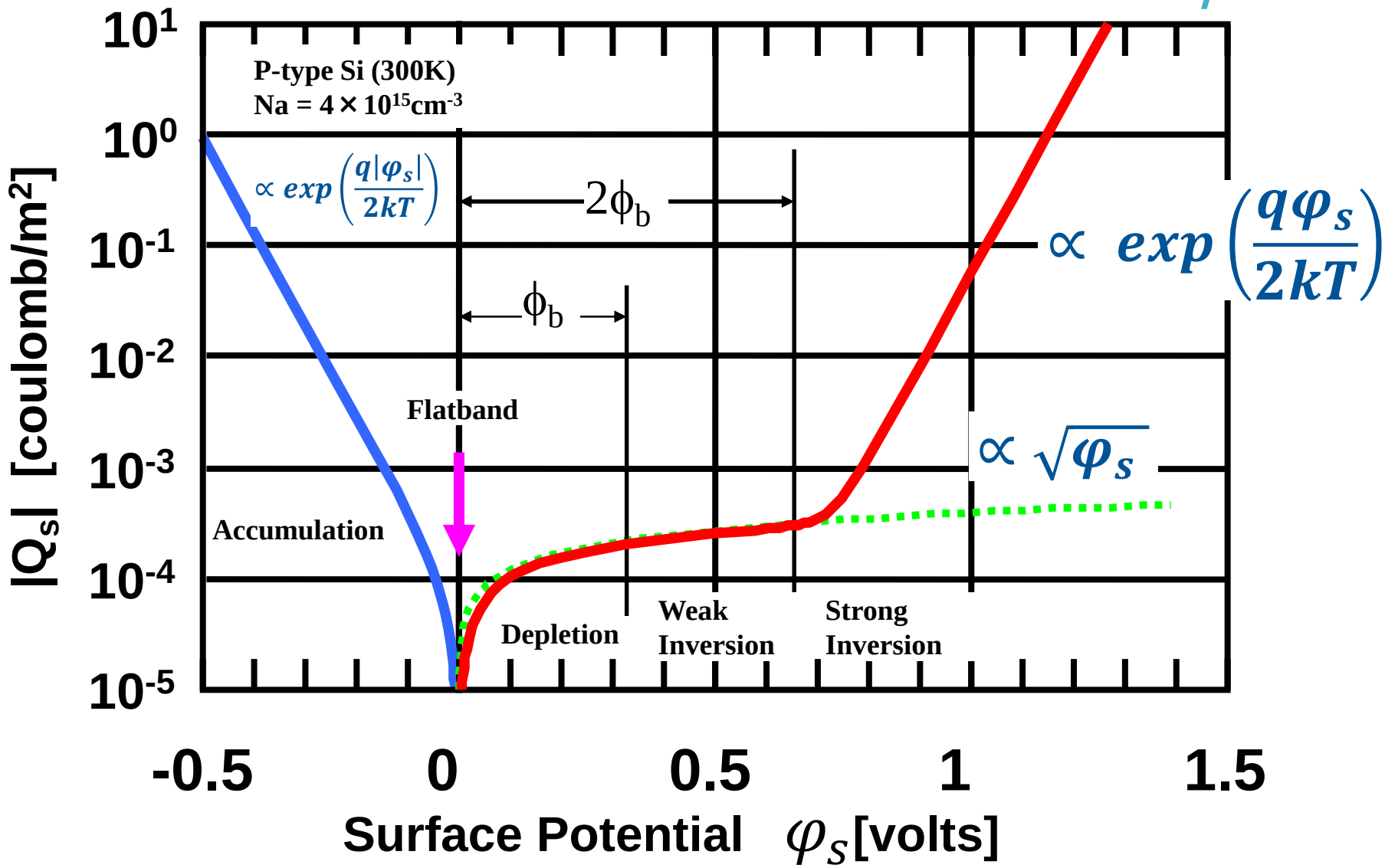
Supplement



Today's summary (1)

- Ideal MOS structure
  - Work functions of the metal and semiconductor is the same.
- In the inversion and the strong inversion, electrons appear in conduction band due to the band bending when the semiconductor is p-type. IF the semiconductor is n-type, holes appear in the valence band.

Today's summary (2)

- At the strong inversion, the surface potential becomes
- The depletion layer width reaches the maximum at the strong inversion.（強反転すると空乏層幅は最大値となる）
- The electrons in the inversion layer is the current of n-channel MOSFET, where the substrate is p-type.（反転層の電子がnチャネルMOSFETにおける電流となる）