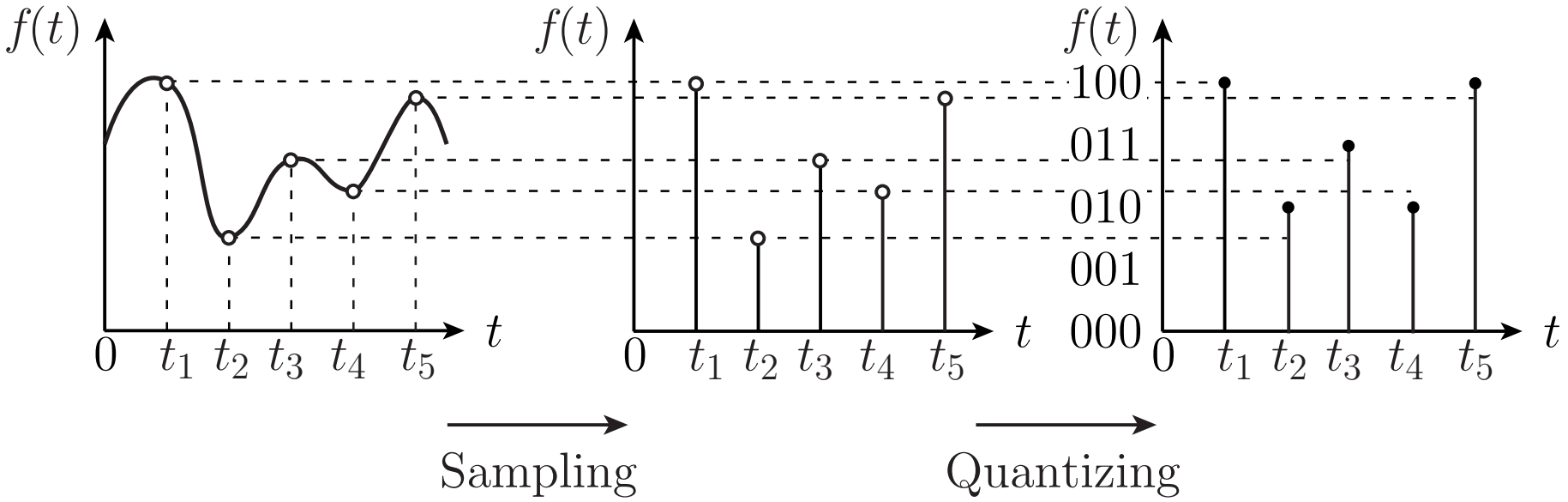
A-D変換器とD-A変換器
現実の世界と理想の世界

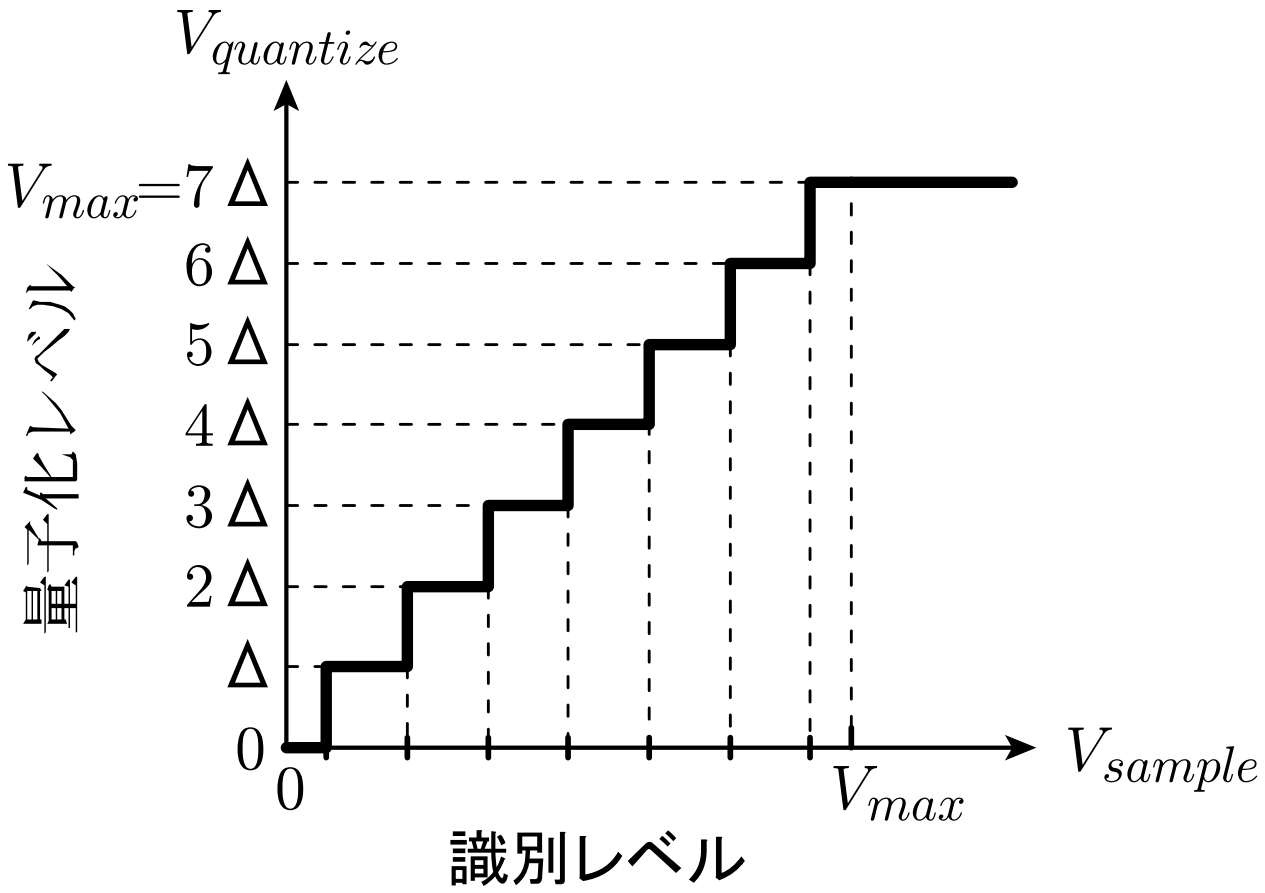
A-D変換器とD-A変換器の概要

アナログ信号：連続振幅　（連続時間）

ディジタル信号：離散時間，離散振幅　（0, 1の数値列）

標本化　　量子化　　符号化





V_{sample} : 標本化したアナログ信号

$V_{quantize}$: V_{sample} を量子化した信号

Δ : 量子化ステップ

V_{max} : フルスケール

$$\Delta = \frac{V_{max}}{2^n - 1}$$

$$V_{quantize}=(b_n\times 2^{n-1}+b_{n-1}\times 2^{n-2}+\cdots+b_2\times 2+b_1)\Delta$$

$V_{quantize}\rightarrow b_n b_{n-1}\cdots b_2 b_1$ ：2進数表示（符号化の1種）

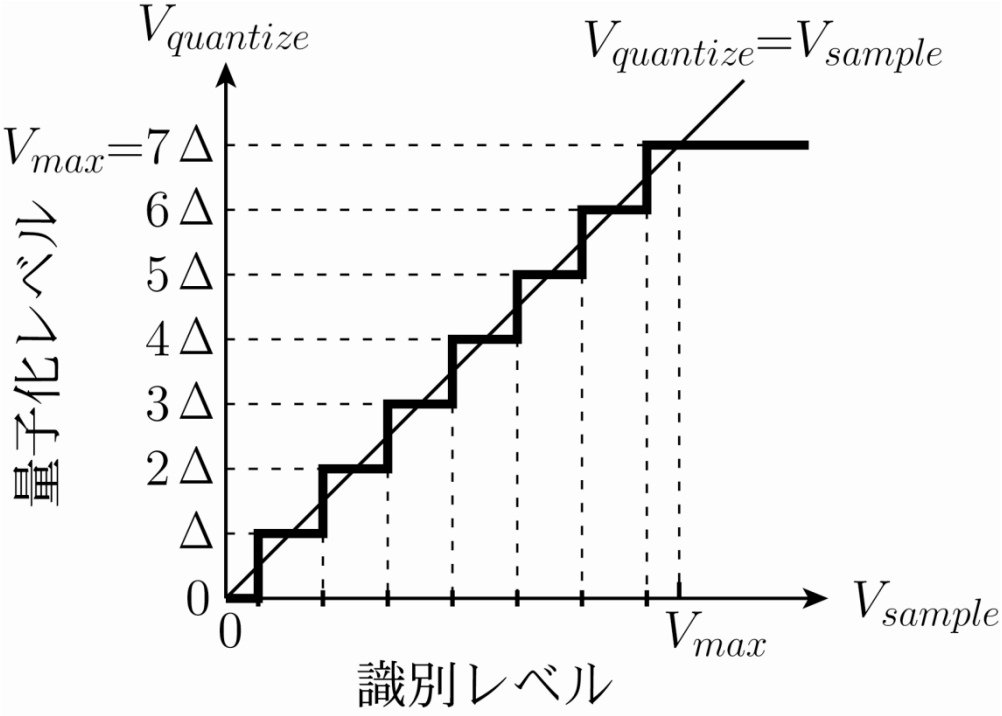
nビットのディジタル信号

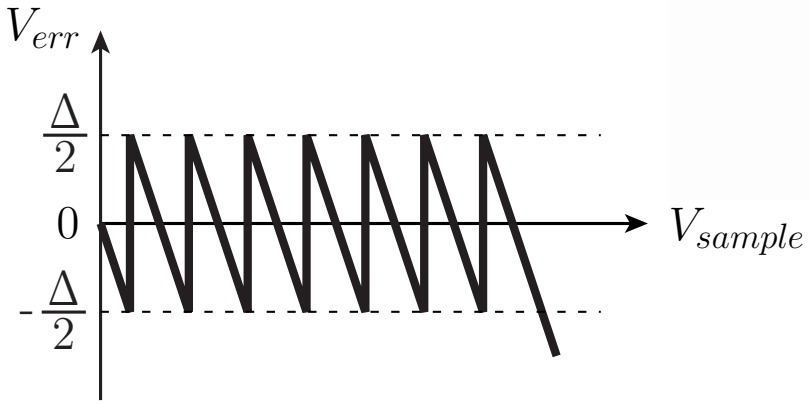
b_n : Most Significant Bit (MSB)

b_1 :Least Significant Bit (LSB)　　$(\Delta=1\mathrm{LSB})$

変換器の評価

量子化雑音





$$p(V_{err})=\frac{1}{\Delta} \quad \left(|V_{err}|\leq\frac{\Delta}{2}\right)$$

$$P_N=\int_{-\Delta/2}^{\Delta/2}p(V_{err}){V_{err}}^2dV_{err}$$

$$=\frac{1}{\Delta}\int_{-\Delta/2}^{\Delta/2}{V_{err}}^2dV_{err}$$

$$=\frac{\Delta^2}{12}$$

信号電力

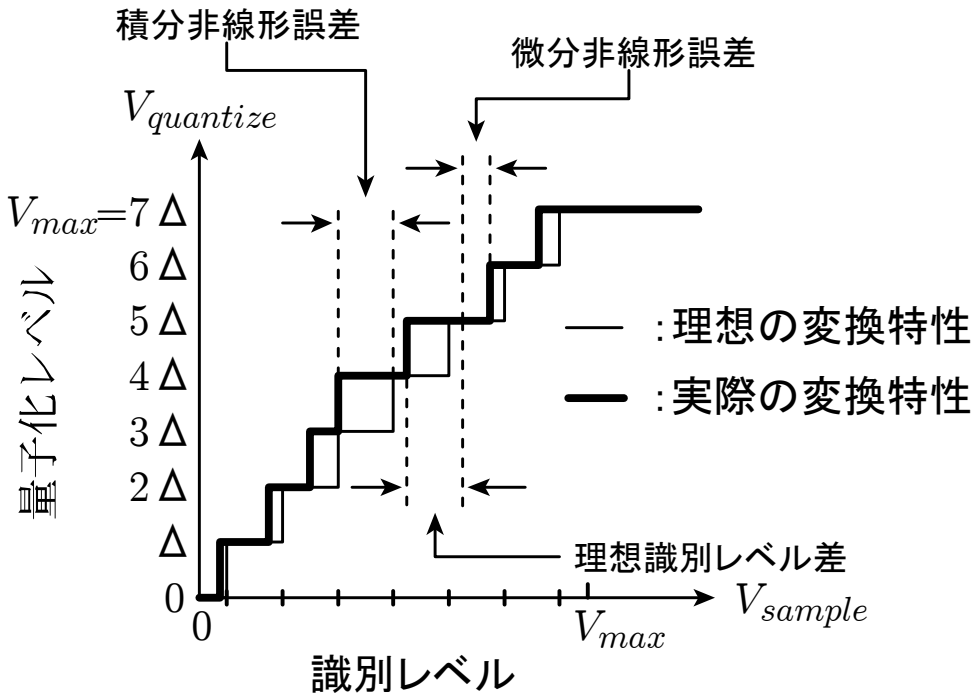
$$P_S = \frac{1}{T}\int_0^T \left\{\frac{V_{max}}{2}\sin(2\pi\frac{t}{T})\right\}^2 dt = \frac{1}{T}\int_0^T \frac{{V_{max}}^2}{4}\cdot\frac{1-\cos(4\pi\frac{t}{T})}{2}dt$$

$$= \frac{{V_{max}}^2}{8} \qquad \left(\Delta = \frac{V_{max}}{2^n - 1}\right)$$

$$SNR_{max} = 10\log\frac{P_S}{P_N} = 10\log\frac{\frac{\{(2^n-1)\Delta\}^2}{8}}{\frac{\Delta^2}{12}} = 10\log\left\{\frac{3}{2}(2^n-1)^2\right\}$$

$$= 10\log\frac{3}{2} + 10\log(2^n-1)^2 \approx 10\log\frac{3}{2} + 10\log 2^{2n}$$

$$\approx 10\log\frac{3}{2} + 20n\log 2 \approx 6.02n + 1.76\,\mathrm{dB}$$



静的特性

積分線形性

微分線形性

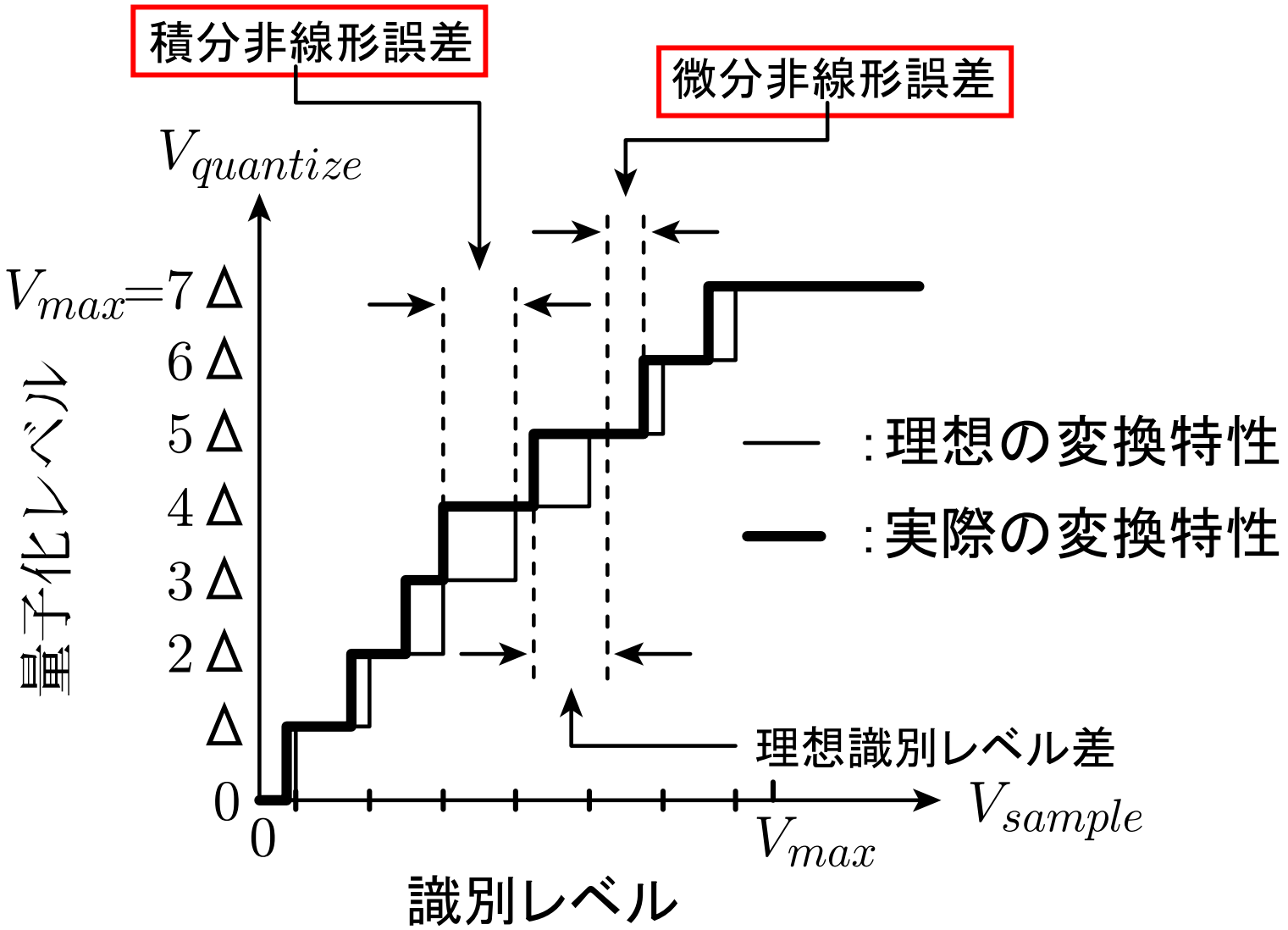
単調性

利得誤差

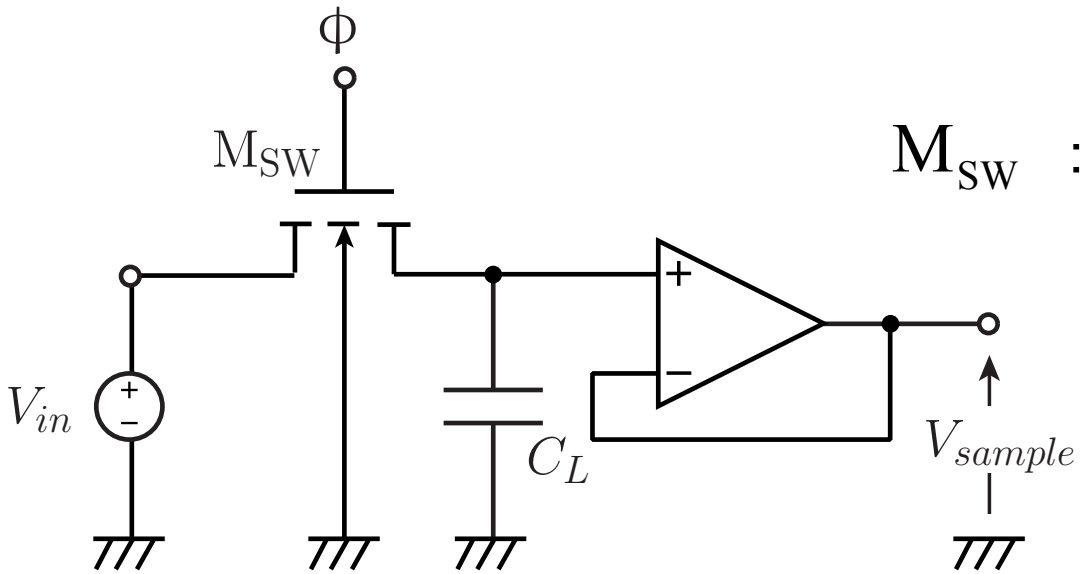
オフセット

動的特性

変換速度（セトリングタイム）

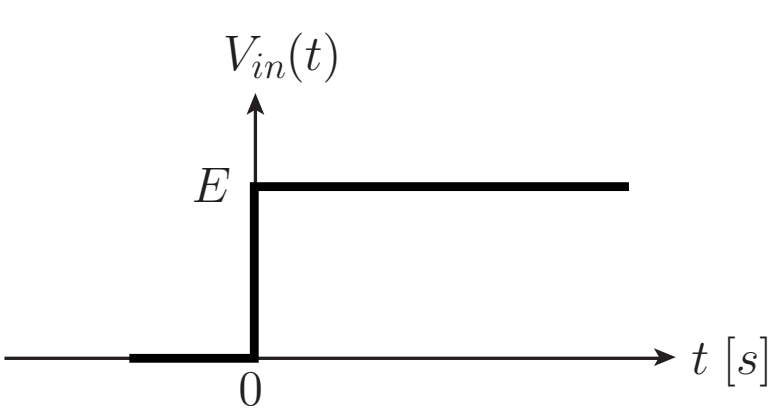

積分非線形誤差
微分非線形誤差
$V_{quantize}$
V_{max}=7Δ
6Δ
5Δ
4Δ
3Δ
2Δ
Δ
0
量子化レベル
0
V_{max}
V_{sample}
識別レベル
:理想の変換特性
:実際の変換特性
理想識別レベル差

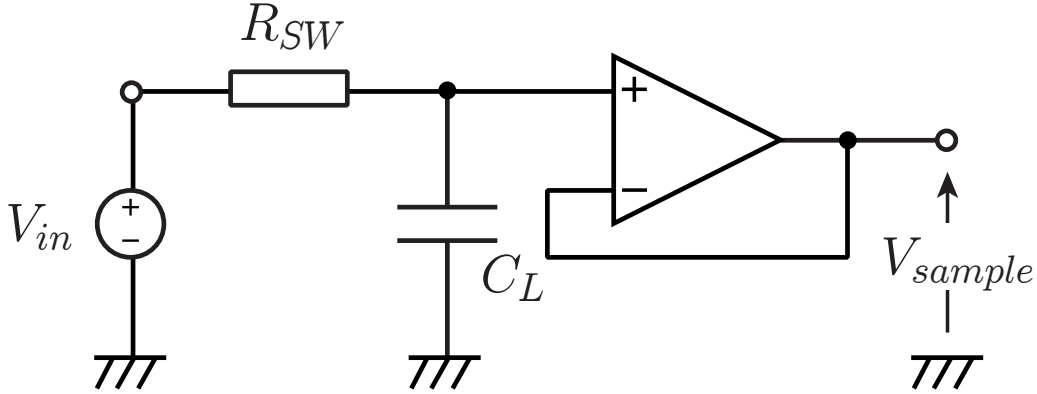
標本化回路の構成



M_{SW}　:スイッチ

M_{SW}の等価抵抗：R_{SW}





$$\frac{V_{in}-V_{sample}}{R_{SW}}=C_L\frac{dV_{sample}}{dt}$$

$t\geq 0$のとき

$$\frac{E}{C_L R_{SW}}=\frac{dV_{sample}}{dt}+\frac{V_{sample}}{C_L R_{SW}}$$

V_{sample}の特殊解は

$$V_{sample}=E$$

$$\frac{dV_{sample}}{dt}+\frac{V_{sample}}{C_L R_{SW}}=0$$の一般解は

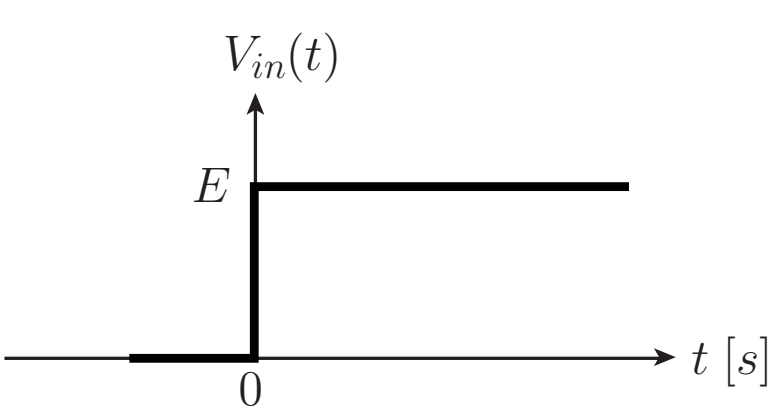
$$V_{sample}=\pm A\exp\left(\frac{-t}{C_L R_{SW}}\right)$$　ただし，Aは正の定数

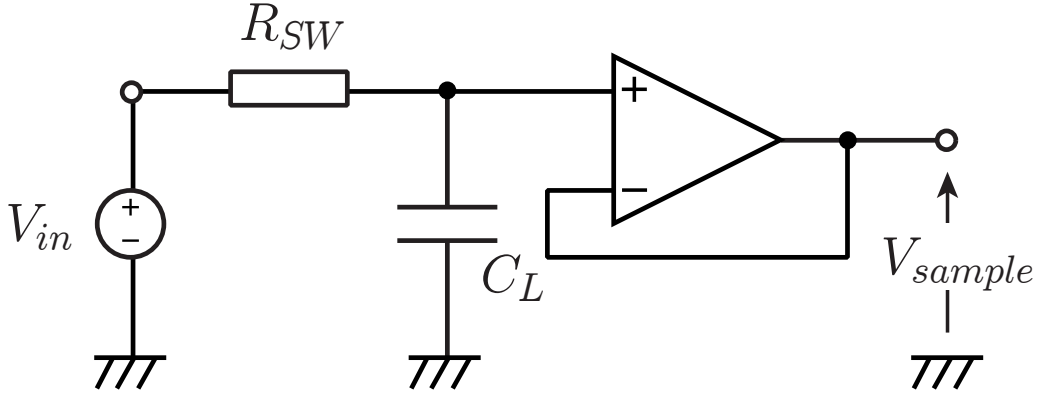
したがって，V_{sample}は

$$V_{sample}=E\pm A\exp\left(\frac{-t}{C_L R_{SW}}\right)$$

$t=0$のときC_Lに蓄えられている電荷を零と仮定

$$V_{sample}=E\left\{1-\exp\left(\frac{-t}{C_L R_{SW}}\right)\right\}$$





$$V_{sample}=E\left\{1-\exp\left(\frac{-t}{C_L R_{SW}}\right)\right\}\text{なので}$$

t_{hold}秒後のV_{sample}

$$V_{sample}=\left\{1-\exp\left(\frac{-t_{hold}}{C_L R_{SW}}\right)\right\}E$$

$$t_{hold} >> C_L R_{SW} \rightarrow V_{sample} \approx V_{in}$$

$t_{hold} >> C_L R_{SW}$

C_L ：寄生容量により定まる下限値

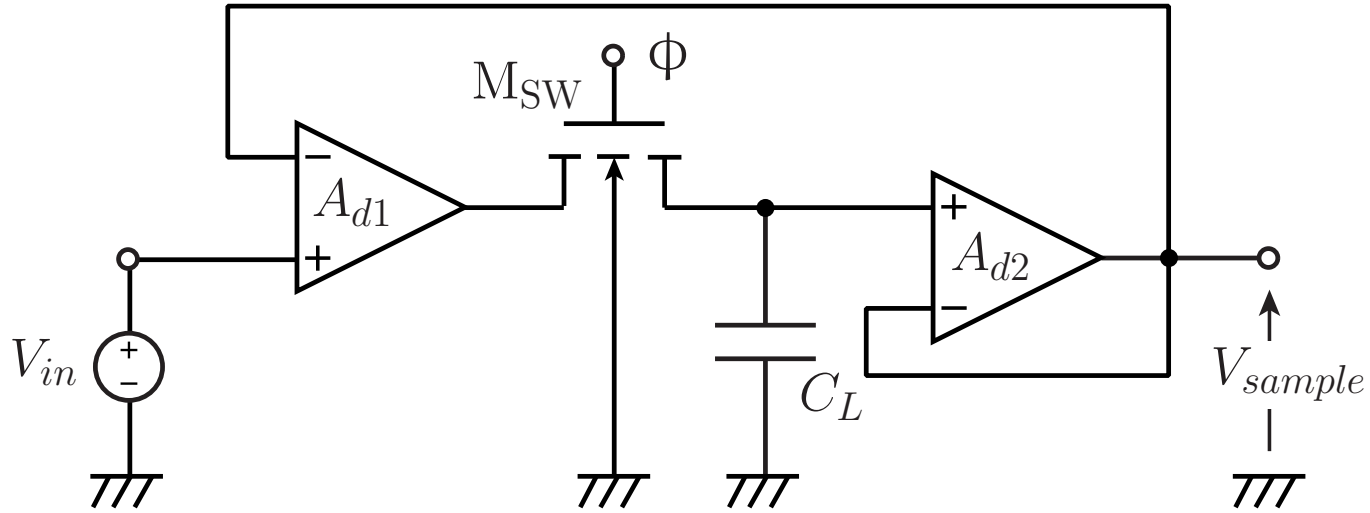
R_{SW} ：許容できるスイッチ $\mathrm{M_{SW}}$ の面積からの下限値

C_Lの増加

↓

回路的な改善

改良した標本化回路



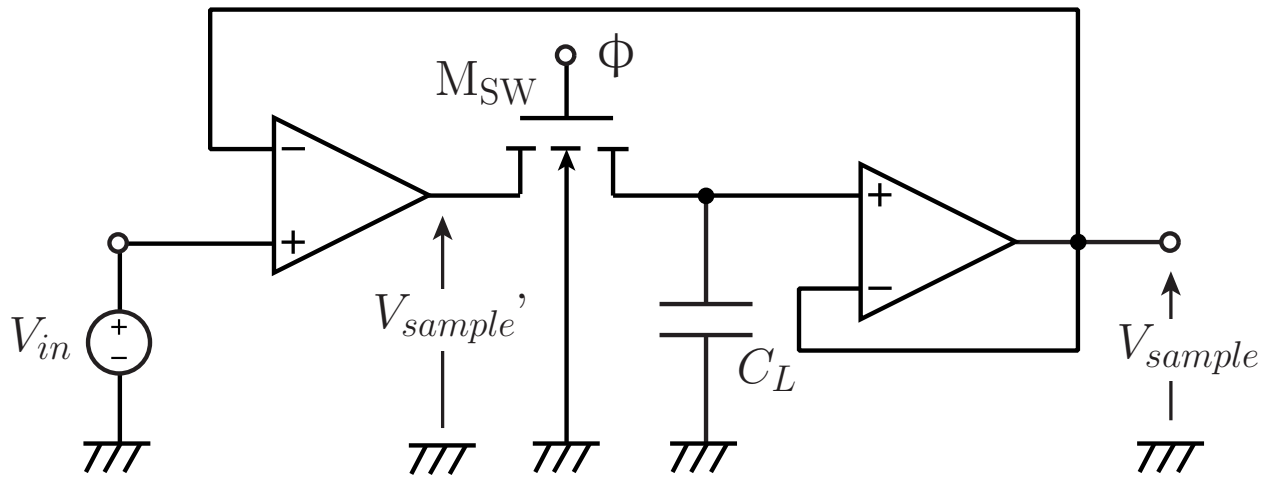
標本化回路(2)

t_{hold} 秒後のV_{sample}

$$V_{sample}=\frac{A_{d1}A_{d2}}{1+A_{d2}+A_{d1}A_{d2}}\left[1-\exp\left\{\frac{-(1+A_{d2}+A_{d1}A_{d2})t_{hold}}{(1+A_{d2})C_L R_{SW}}\right\}\right]E$$

$$C_L R_{SW}\rightarrow(1+A_{d2})C_L R_{SW}/(1+A_{d2}+A_{d1}A_{d2})$$

改良した標本化回路の問題点

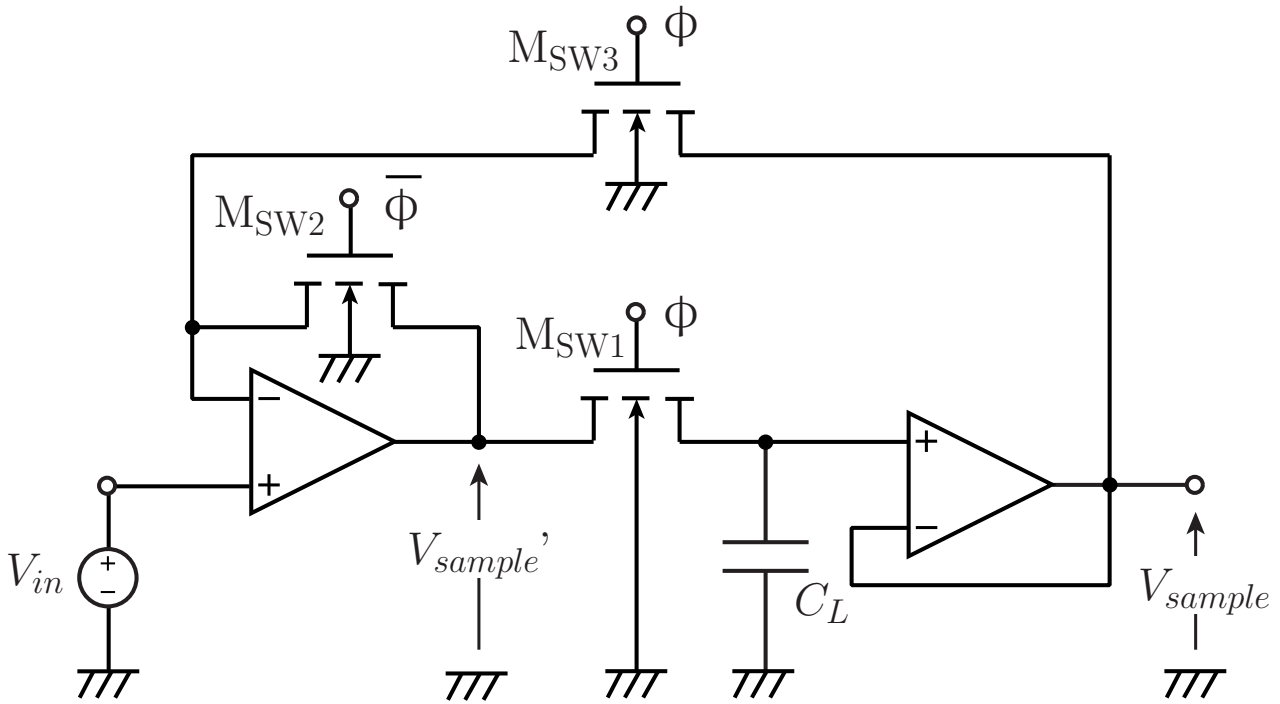


V_{sample}'=V_{DD}または–V_{SS}

↓

V_{sample}' が V_{in} になるまでの時間が大

さらに改良した標本化回路



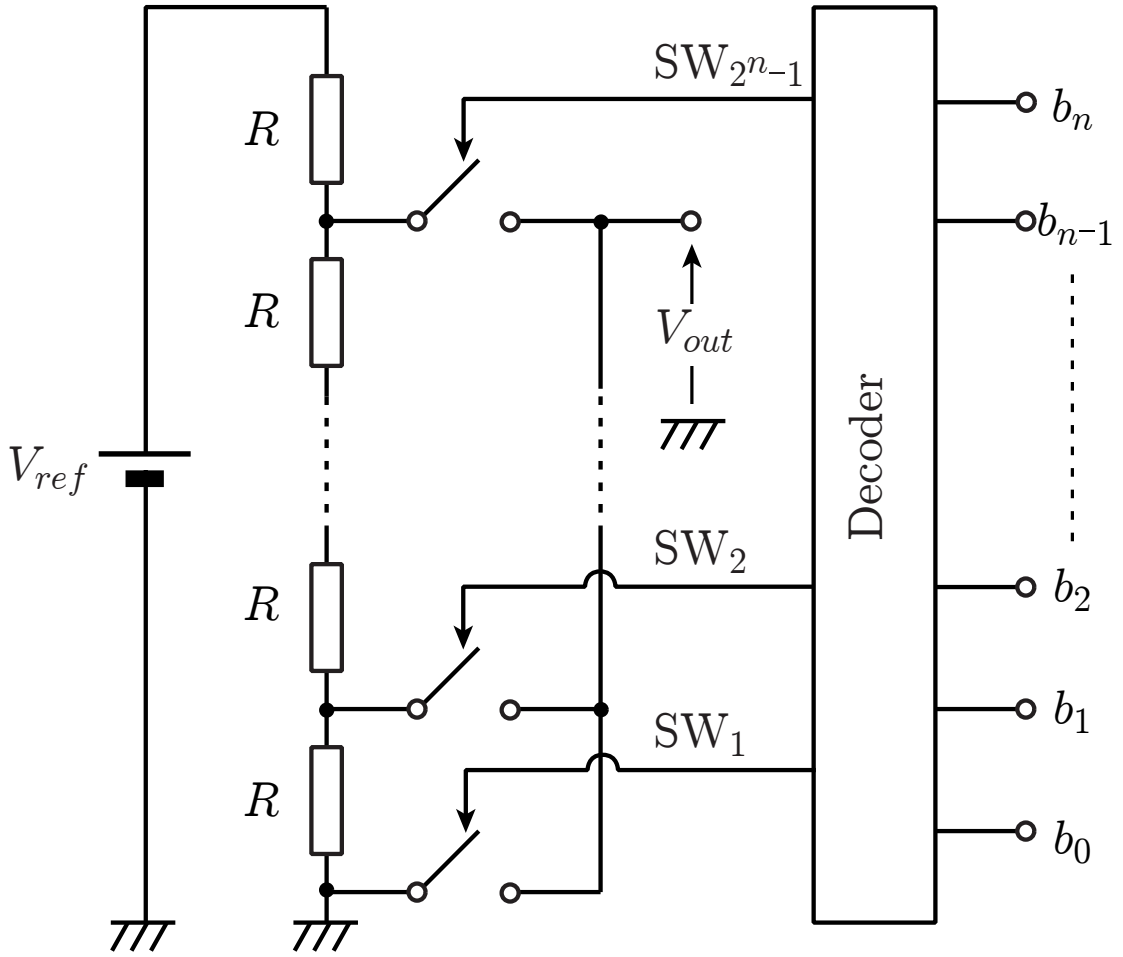
標本化回路(3)

$$V_{sample}' = V_{in}$$

D-A変換器の構成

- 抵抗切り替え型構成
- 電流源切り替え型
- 容量切り替え型
- その他

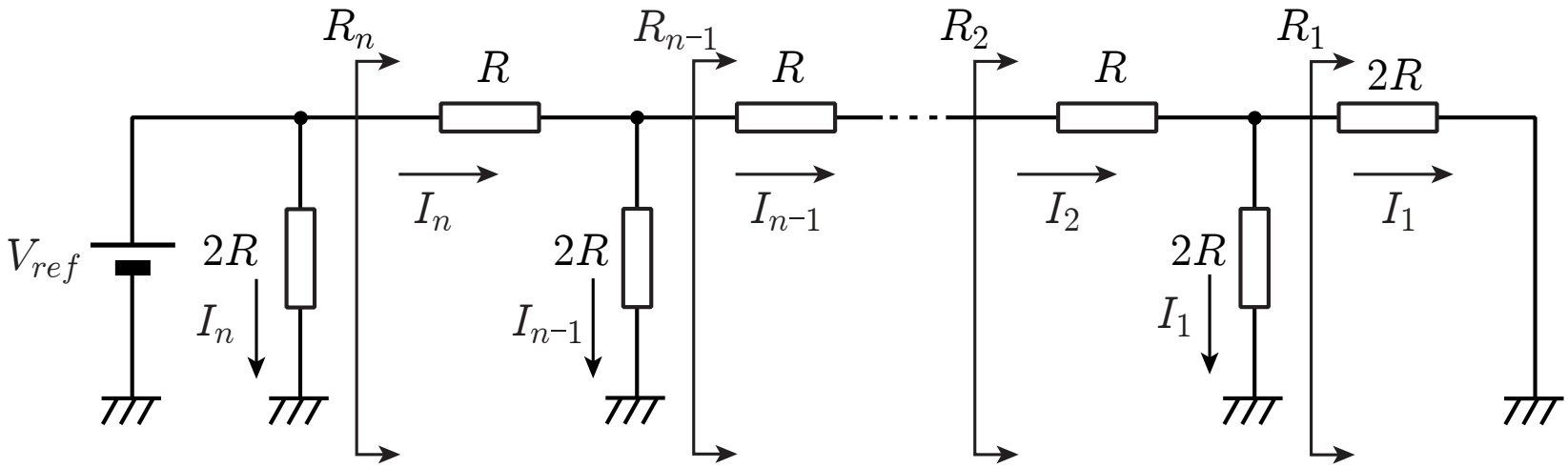
抵抗ストリング構成



$$V_{out} = \frac{i}{2^n} V_{ref} \qquad (i = 0 \text{ to } 2^{n-1}+1)$$

抵抗の面積: $(2^n - 1)R$

R-2R型構成

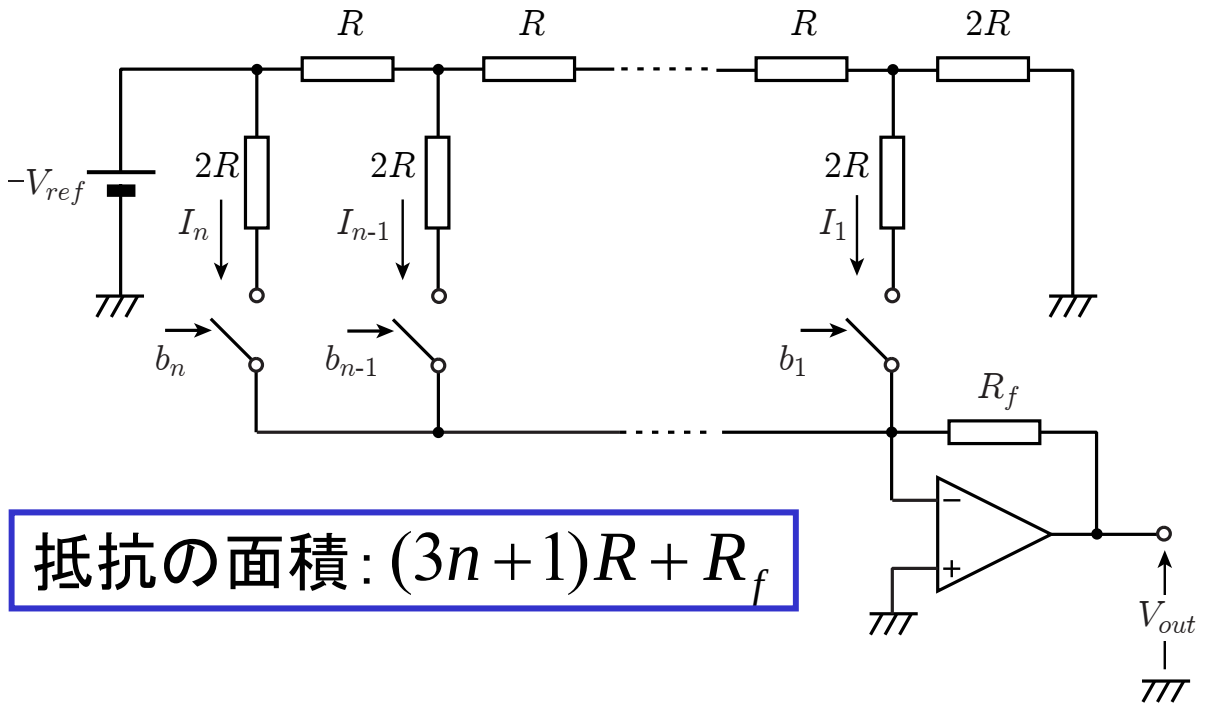


$$R_i = 2R \ (i = 1 \text{ to } n)$$

$$I_{i-1} = \frac{1}{2} I_i \ (i = 2 \text{ to } n)$$

$$I_n = \frac{V_{ref}}{2R}$$

$$V_{quantize}=(b_n\times 2^{n-1}+b_{n-1}\times 2^{n-2}+\cdots+b_2\times 2+b_1)\Delta$$



抵抗の面積 : $(3n+1)R+R_f$

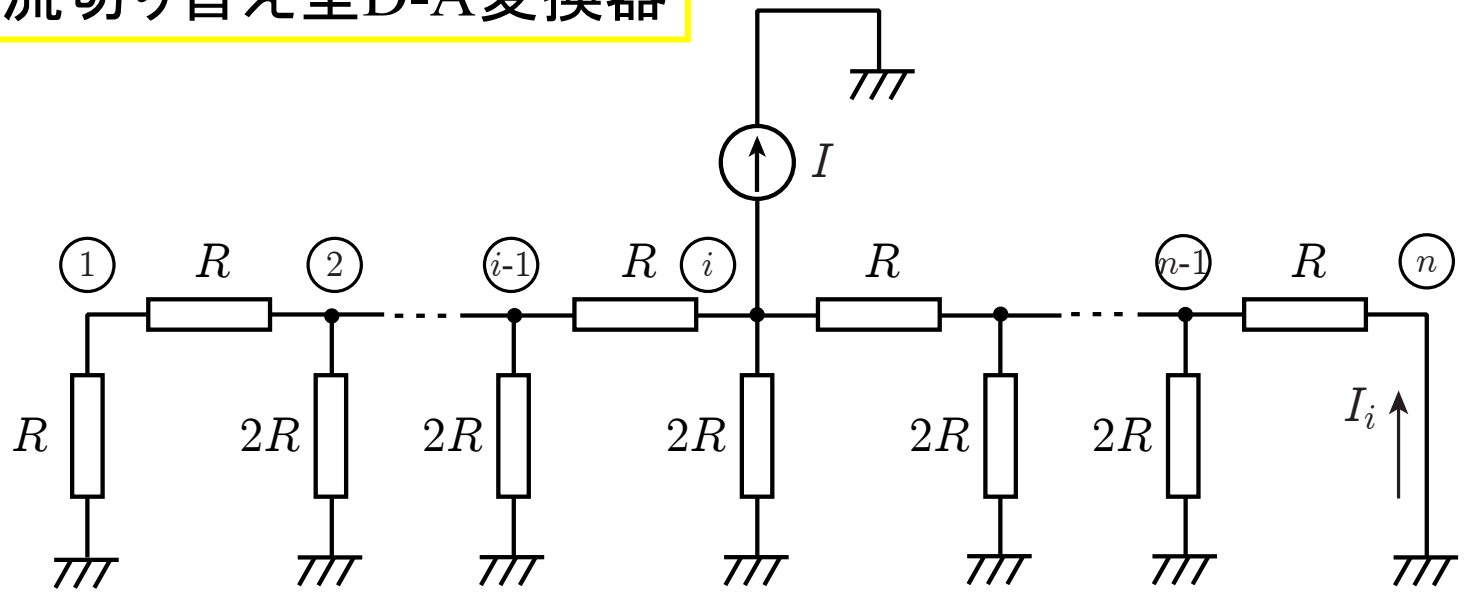
$$V_{out}=-(b_n\times I_n+b_{n-1}\times I_{n-1}+\cdots+b_2\times I_2+b_1\times I_1)R_f$$

$$=-(b_n\times I_n+b_{n-1}\times 2^{-1}I_n+\cdots+b_2\times 2^{-(n-2)}I_n+b_1\times 2^{-(n-1)}I_n)R_f$$

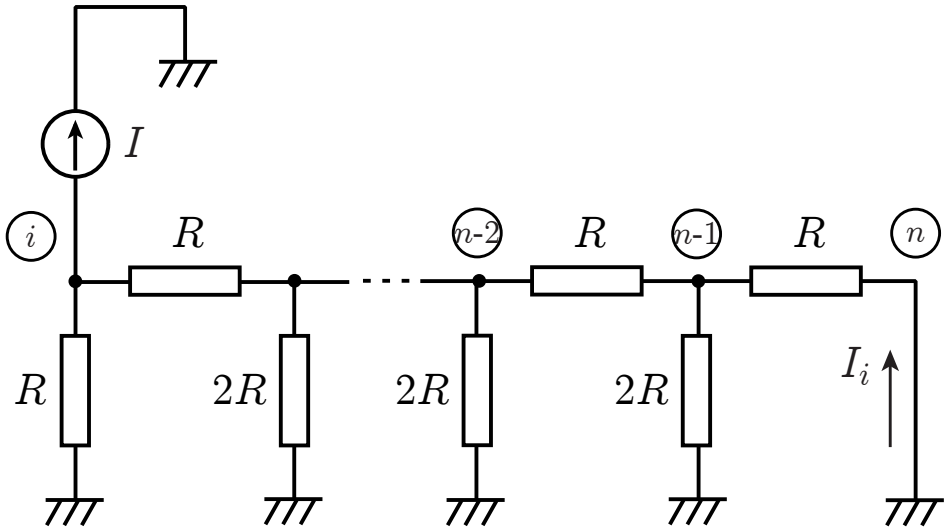
$$=(b_n+b_{n-1}\times 2^{-1}+\cdots+b_2\times 2^{-(n-2)}+b_1\times 2^{-(n-1)})\frac{R_f}{2R}V_{ref}$$

$$=(b_n\times 2^{n-1}+b_{n-1}\times 2^{n-2}+\cdots+b_2\times 2+b_1)\frac{R_f}{2^nR}V_{ref}$$

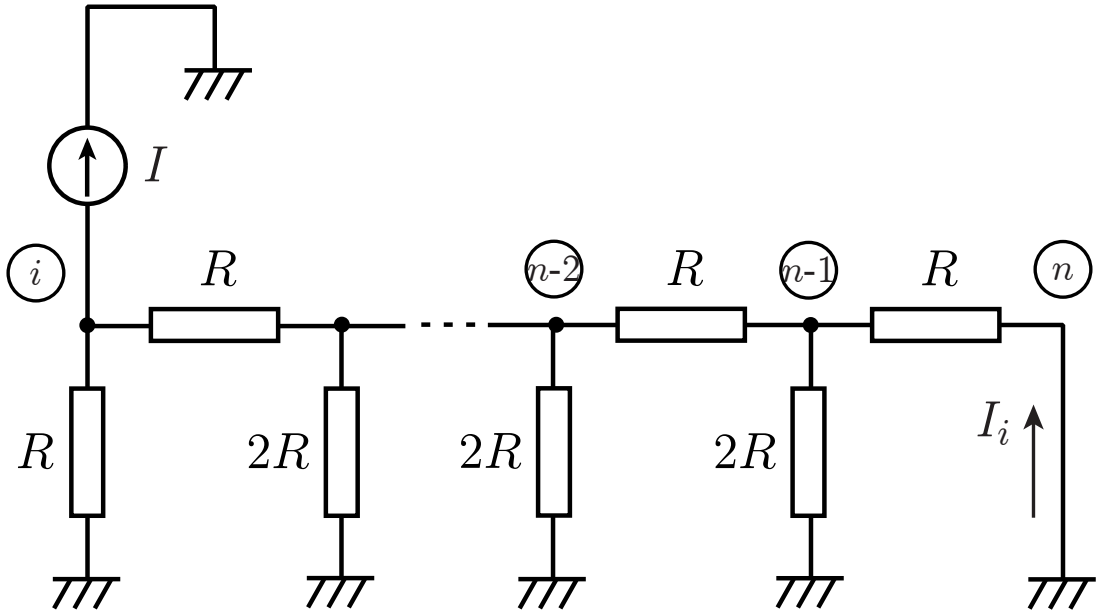
電流切り替え型D-A変換器



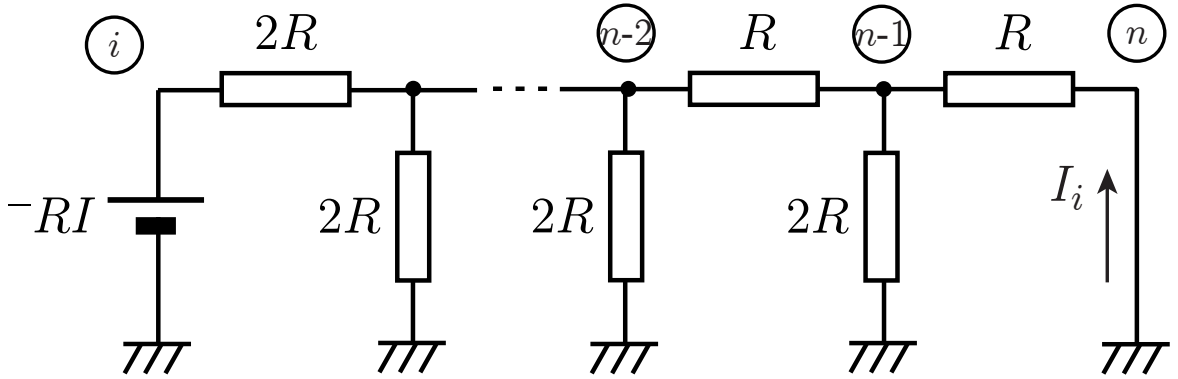
(a)



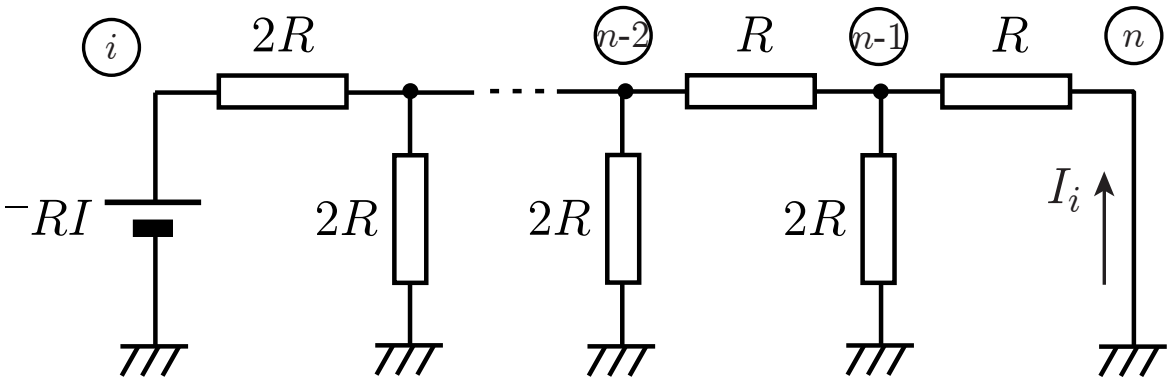
(b)



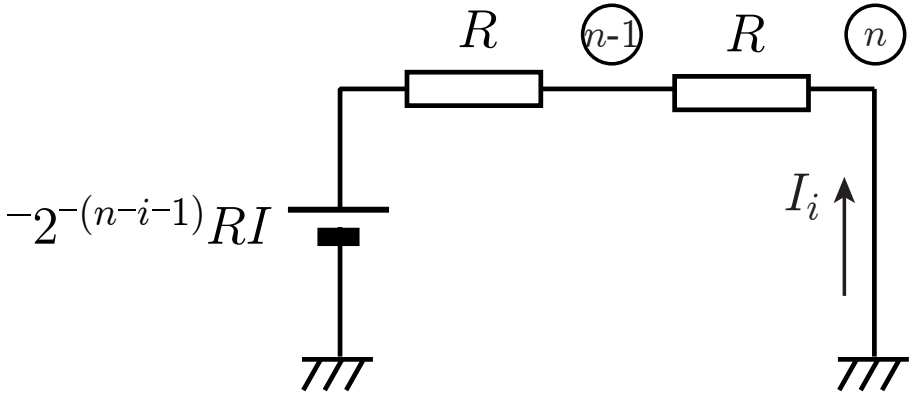
(b)



(c)



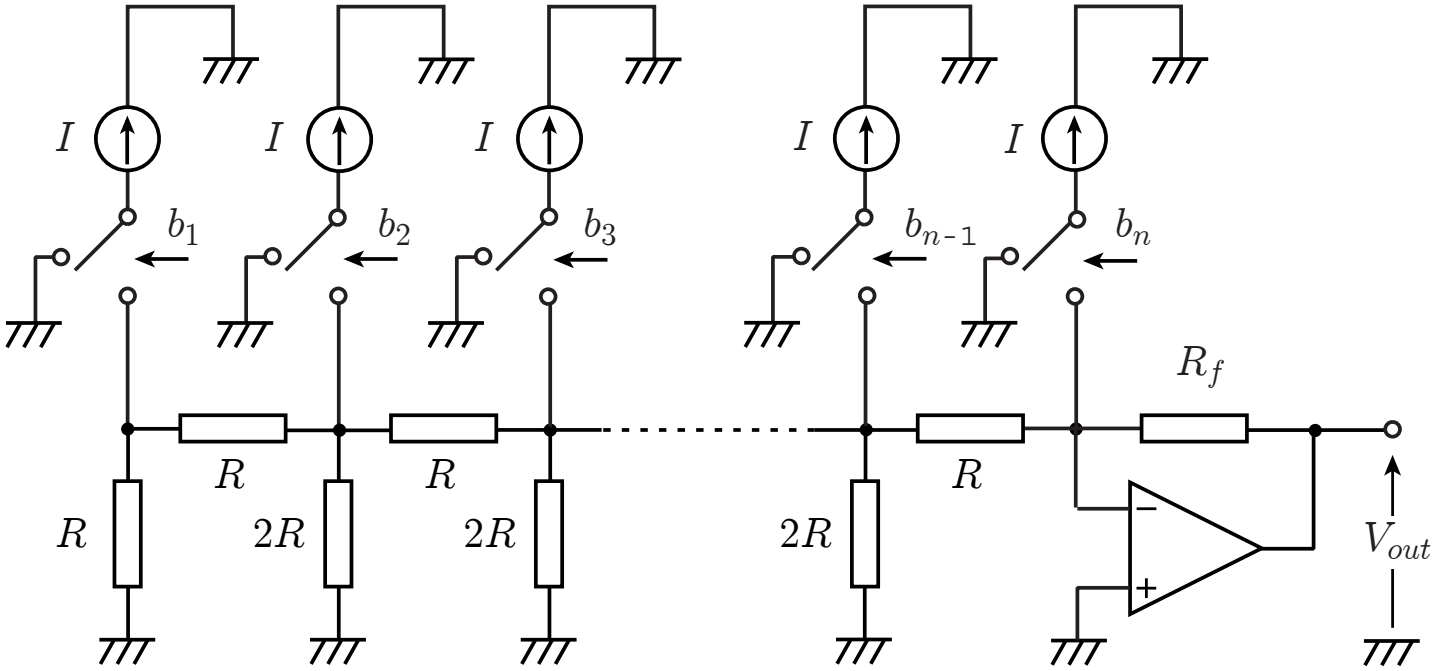
(c)



(d)

$I_n=\frac{V_{ref}}{2R}$とすると

$$I_i=2^{-(n-i)}\frac{V_{ref}}{R}(i=1 \text{ to } n)$$

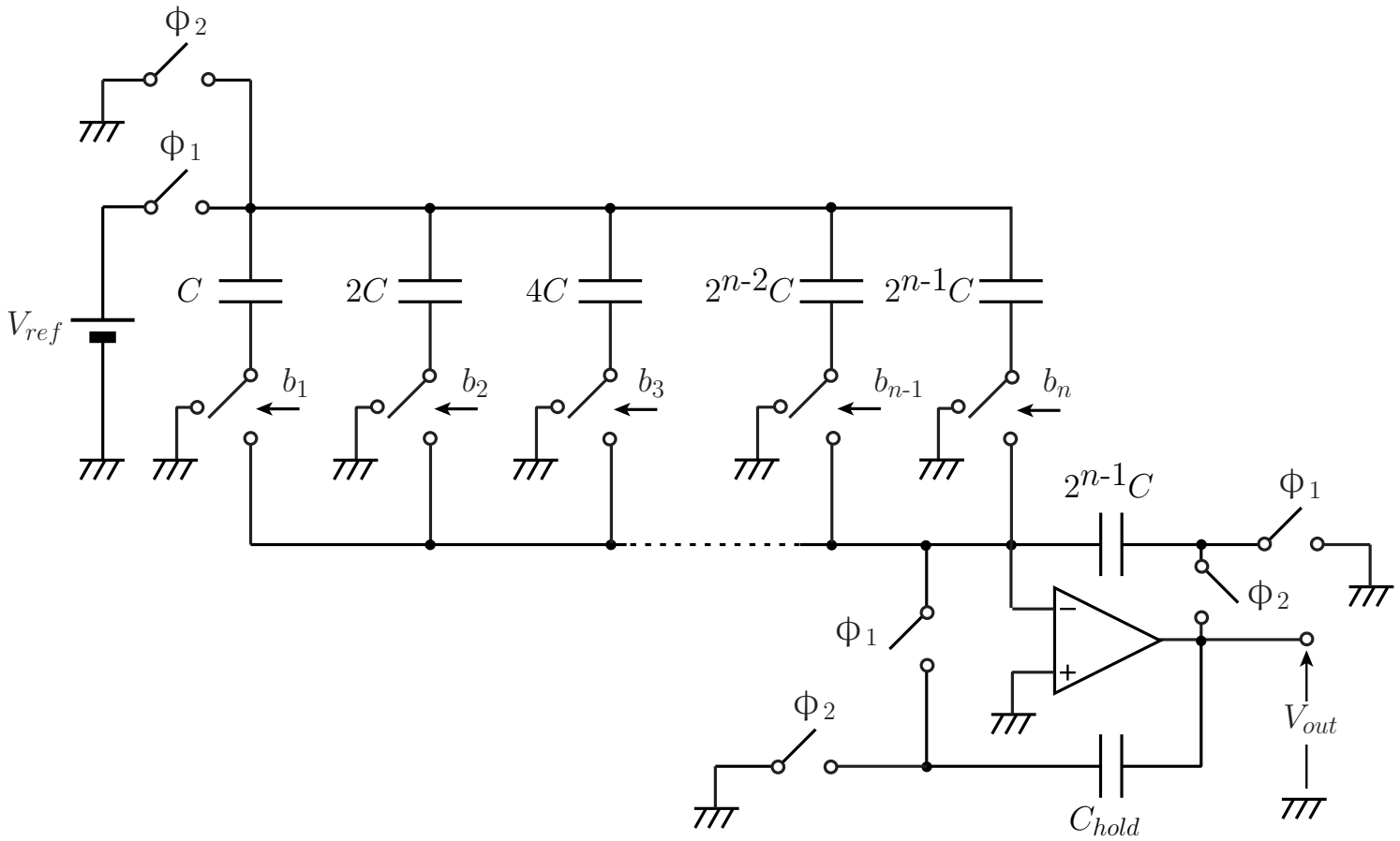


$$V_{out}=(b_n\times 2^{n-1}+b_{n-1}\times 2^{n-2}+\cdots+b_2\times 2+b_1)\frac{R_f}{2^{n-1}R}V_{ref}$$

抵抗の面積: $(3n-1)R+R_f$

スイッチによる電圧降下の影響を受けない

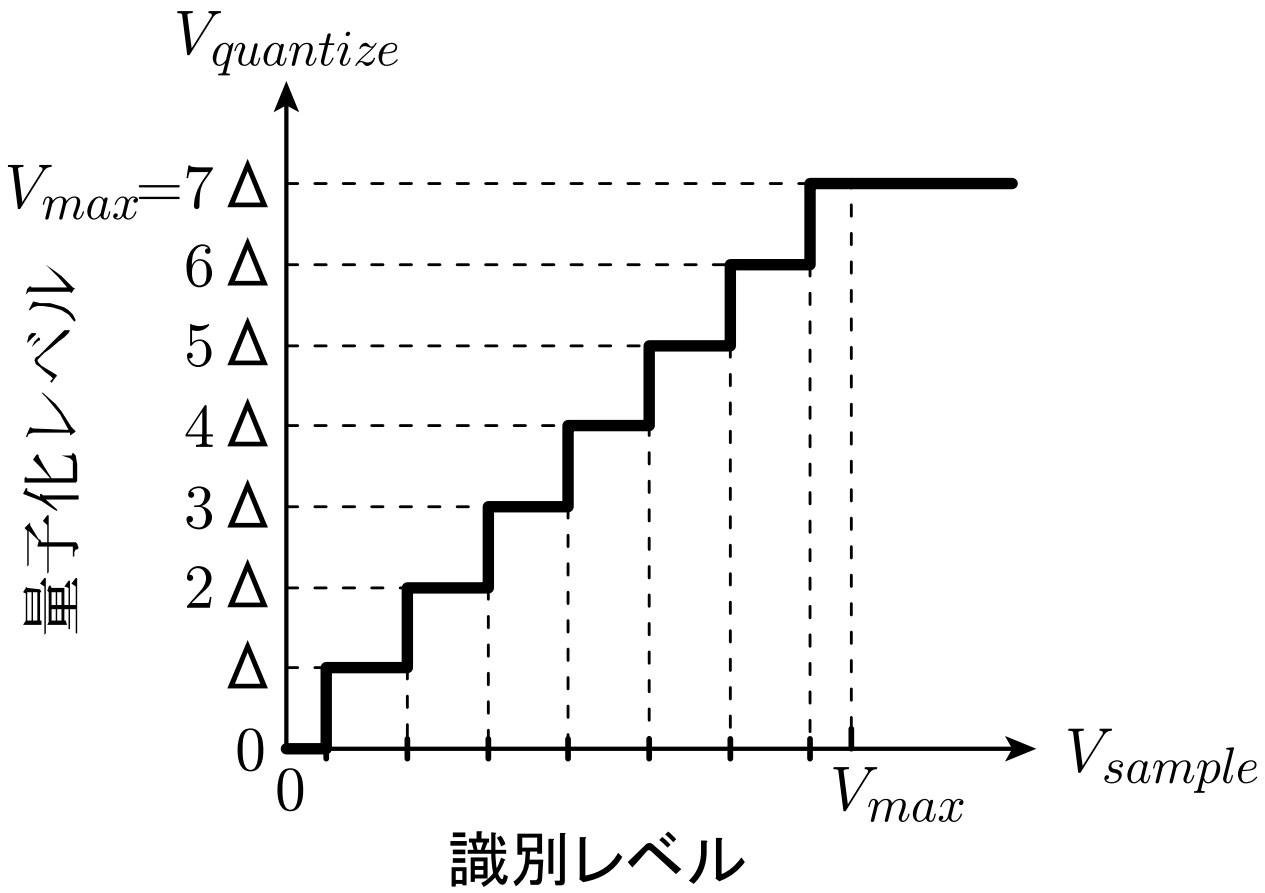
容量切り替え型



スイッチの電圧降下による誤差

MOSプロセスにより容易に実現

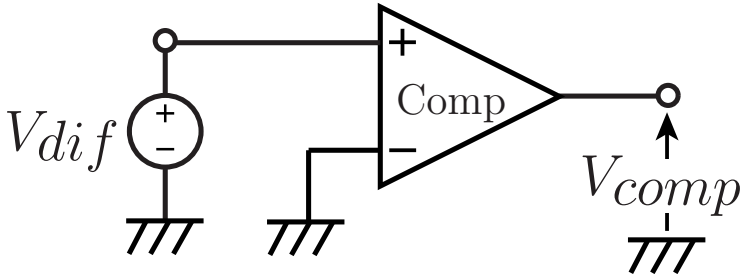
A-D変換器の構成



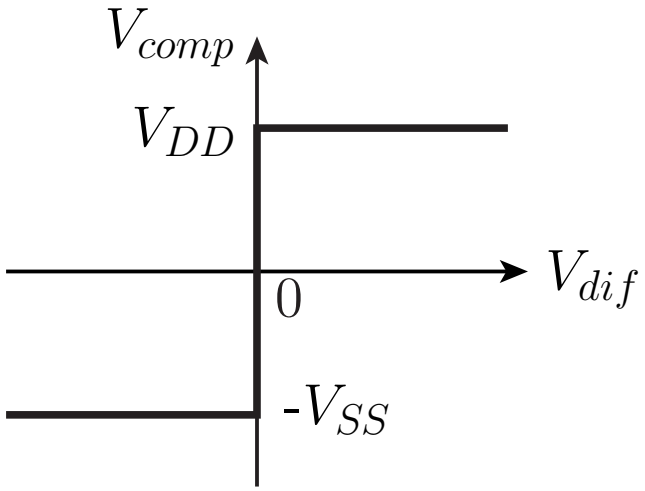
標本値を量子化→比較

比較器の構成

比較器の記号と理想特性

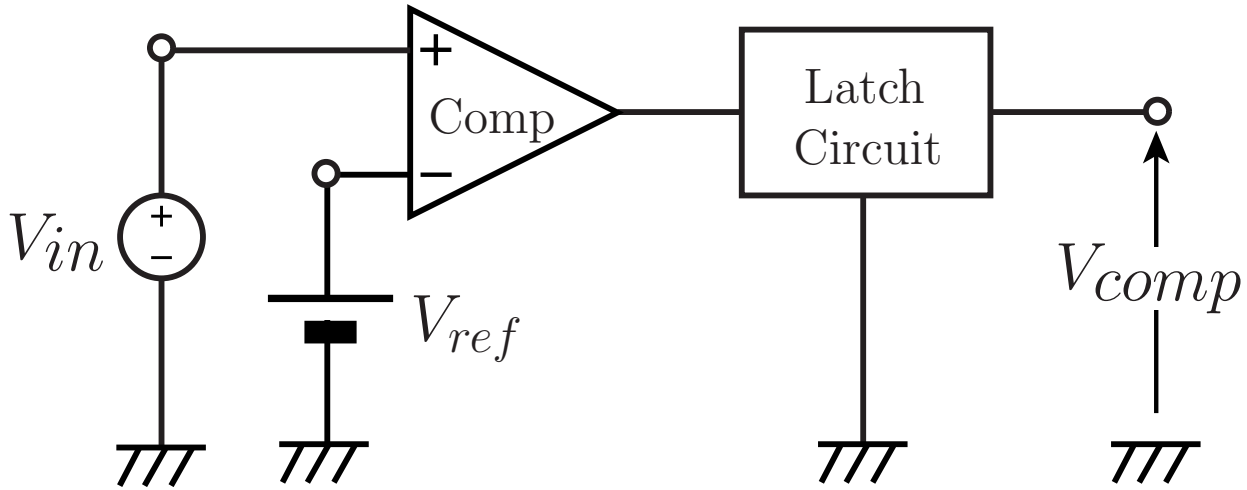


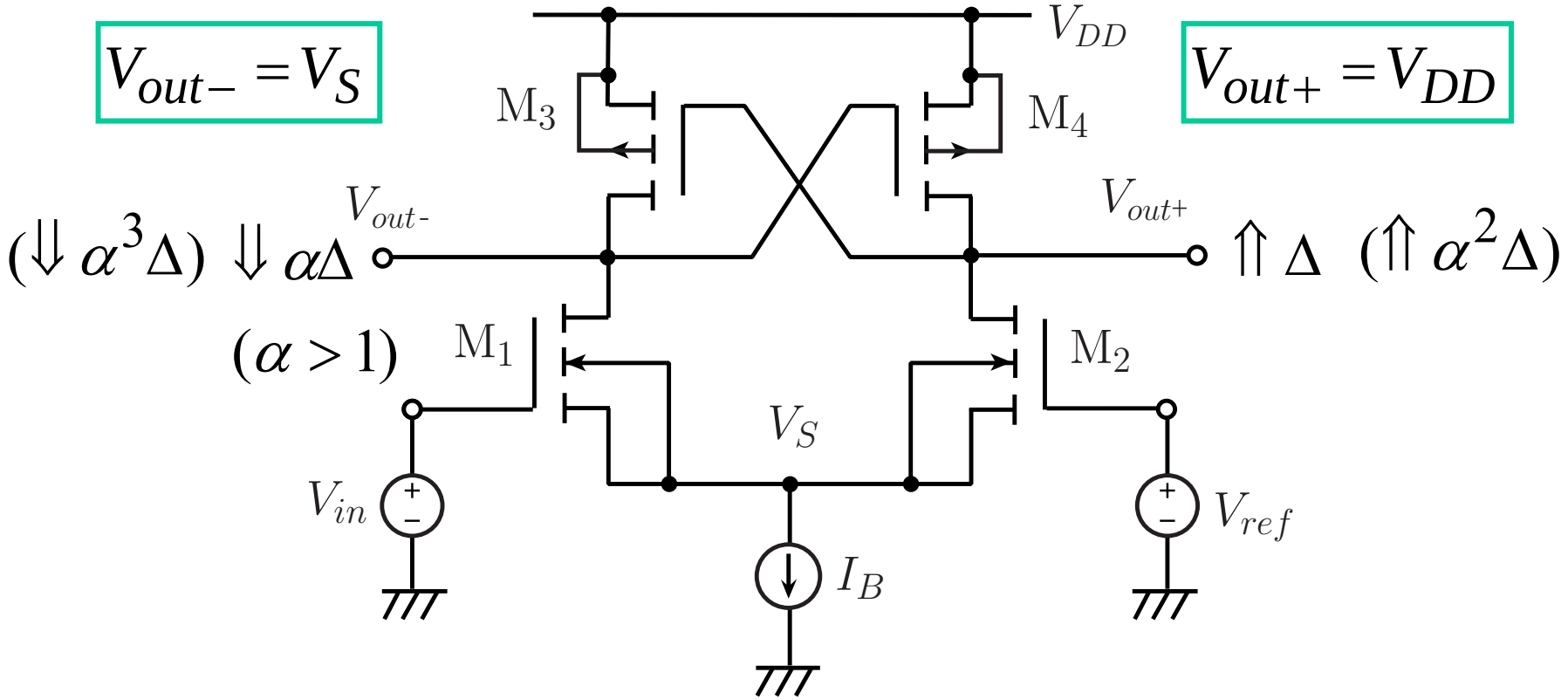
(a)



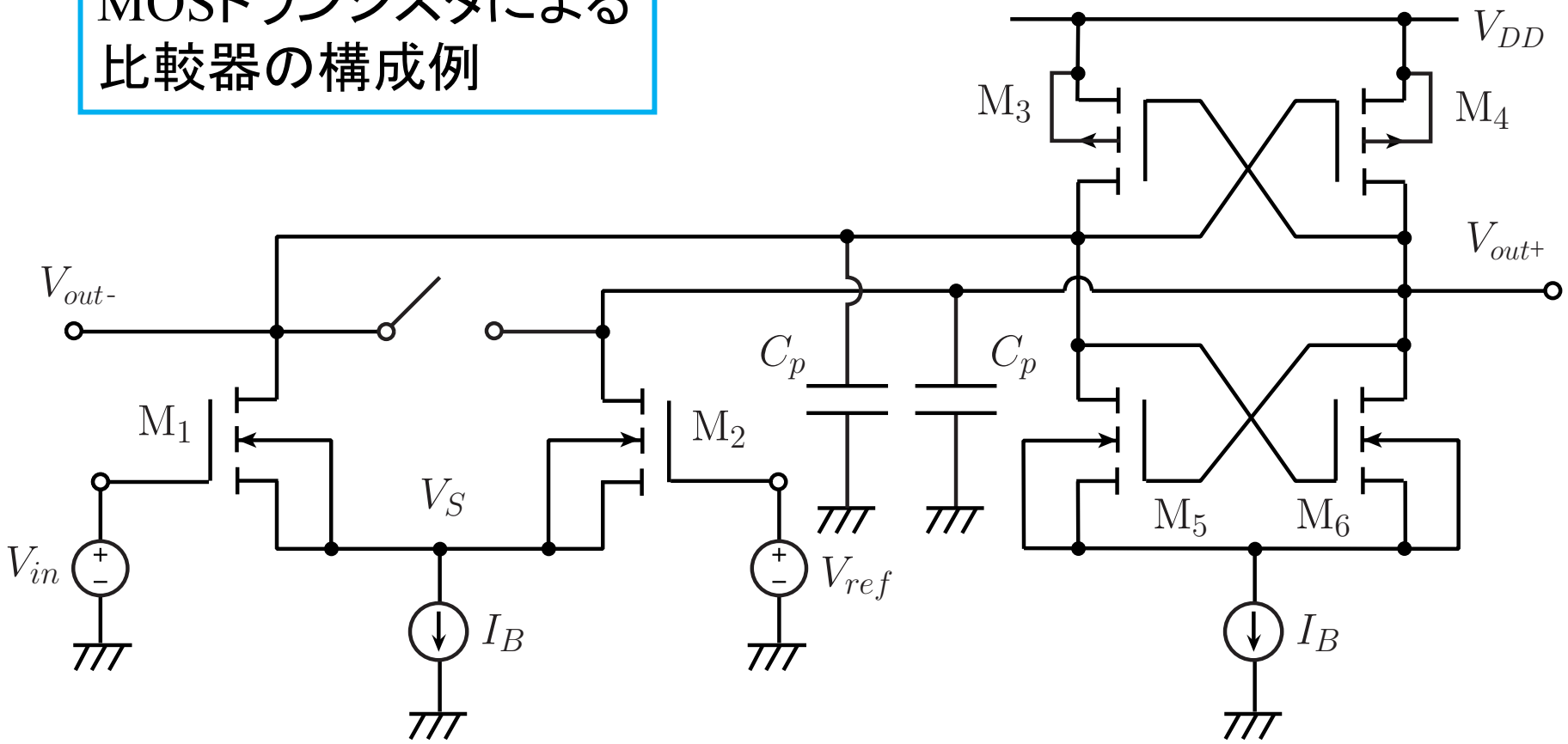
(b)

比較器の動作原理

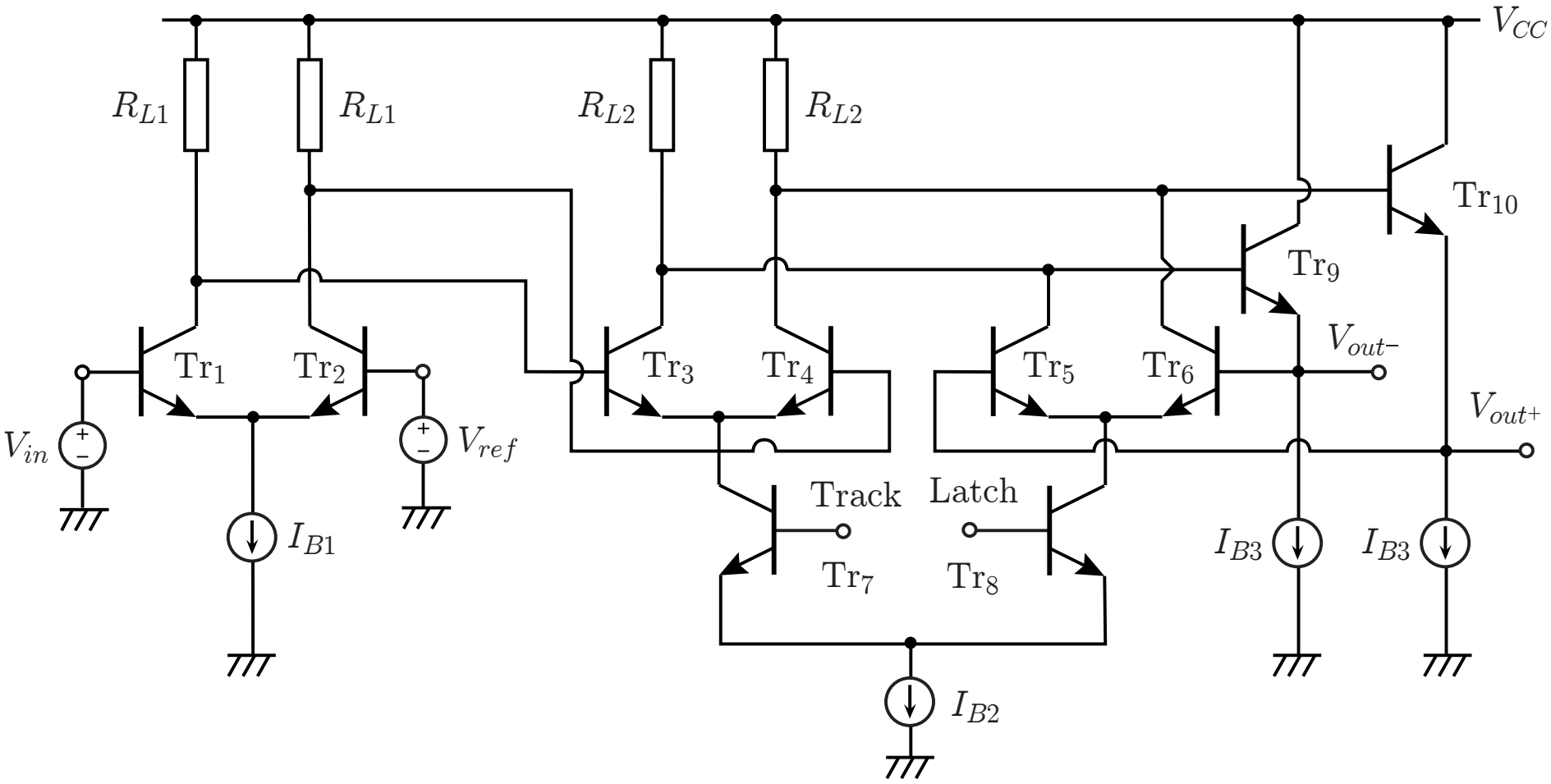



$V_{out-} = V_S$
$V_{out+} = V_{DD}$
V_{DD}
M3
M4
V_{out-}
V_{out+}
$(\Downarrow \alpha^3\Delta) \Downarrow \alpha\Delta$
$\Uparrow \Delta \ (\Uparrow \alpha^2\Delta)$
$(\alpha > 1)$
M1
M2
V_S
V_{in}
V_{ref}
I_B

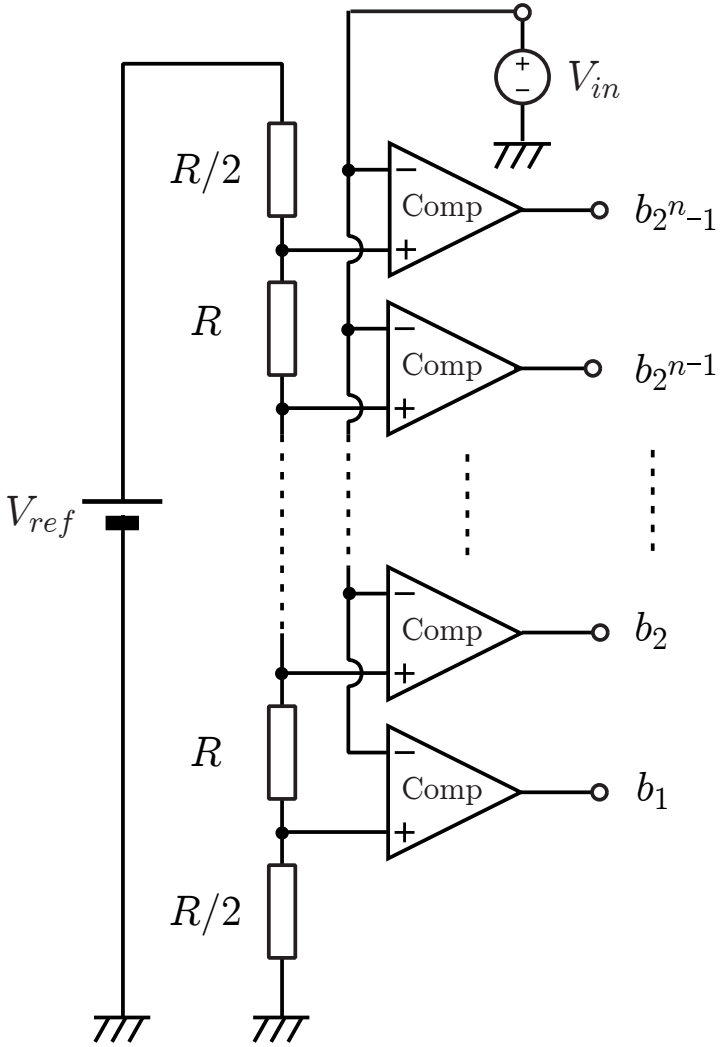
MOSトランジスタによる比較器の構成例

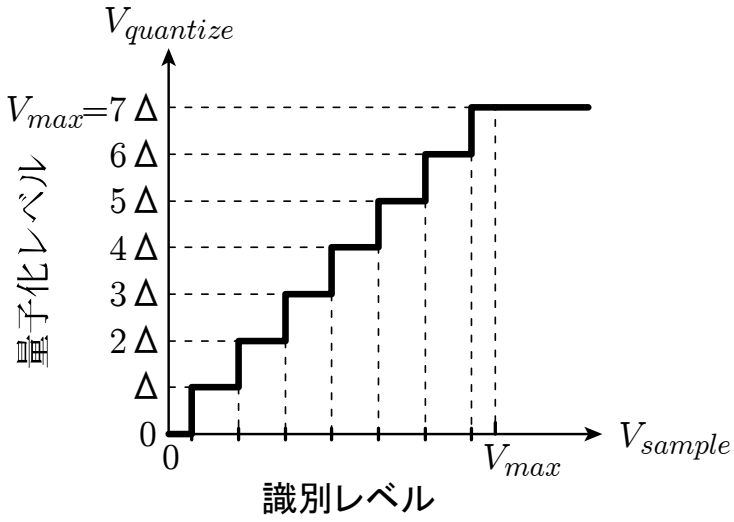


バイポーラトランジスタによる比較器の構成例



フラッシュ型構成



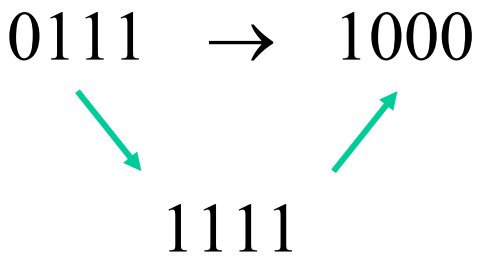


サーモメータコード

高速動作

素子数の指数的増加

グリッチ

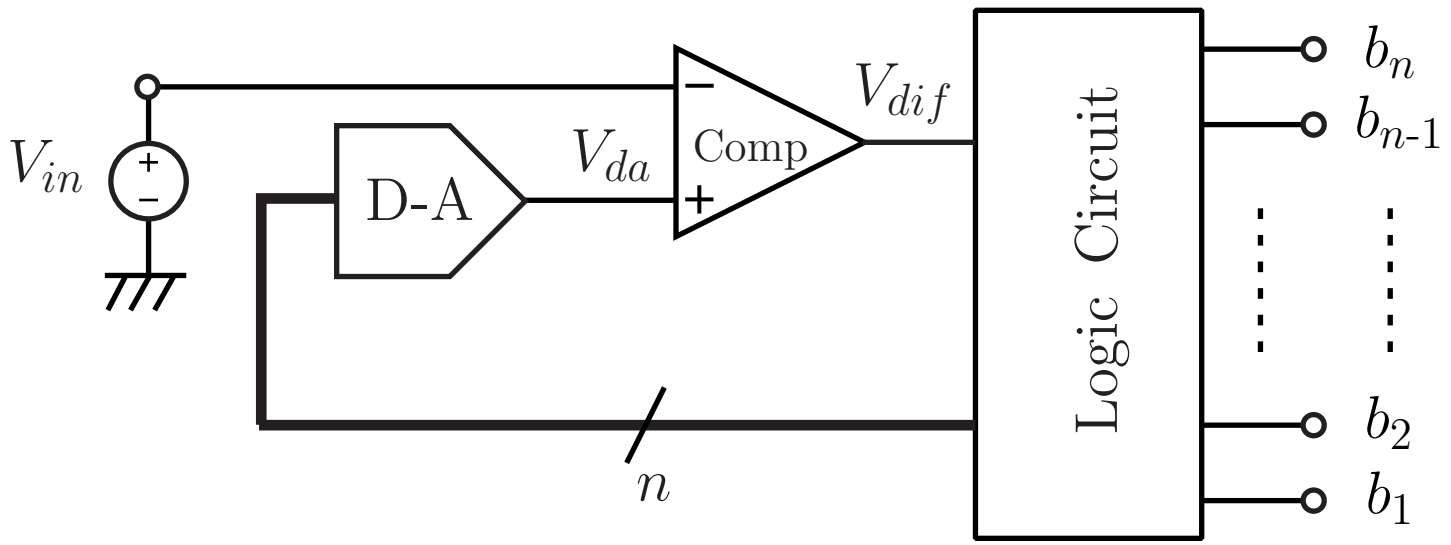


2進数　　サーモメータコード

0111 → 0000000011111111

逐次比較型構成

誤差信号 $\leq \frac{\Delta}{2}$

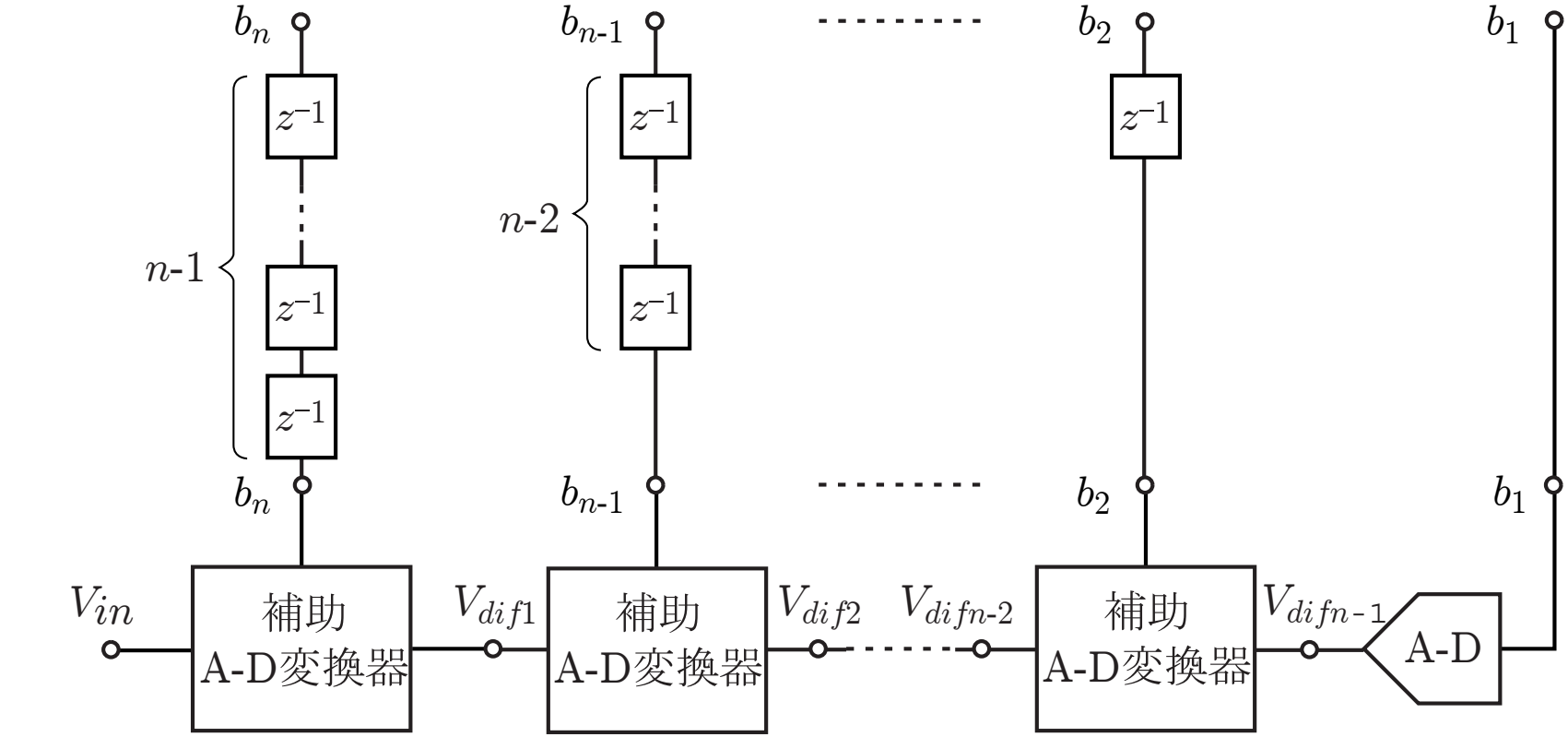


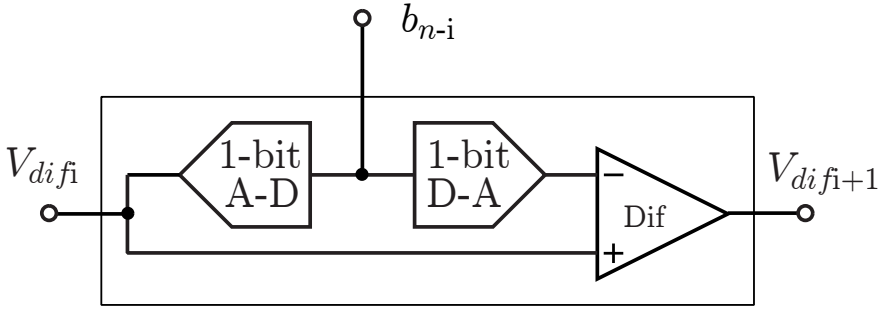
nビットのバス

低速動作

素子数のゆるやかな増加

パイプライン型A-D変換器

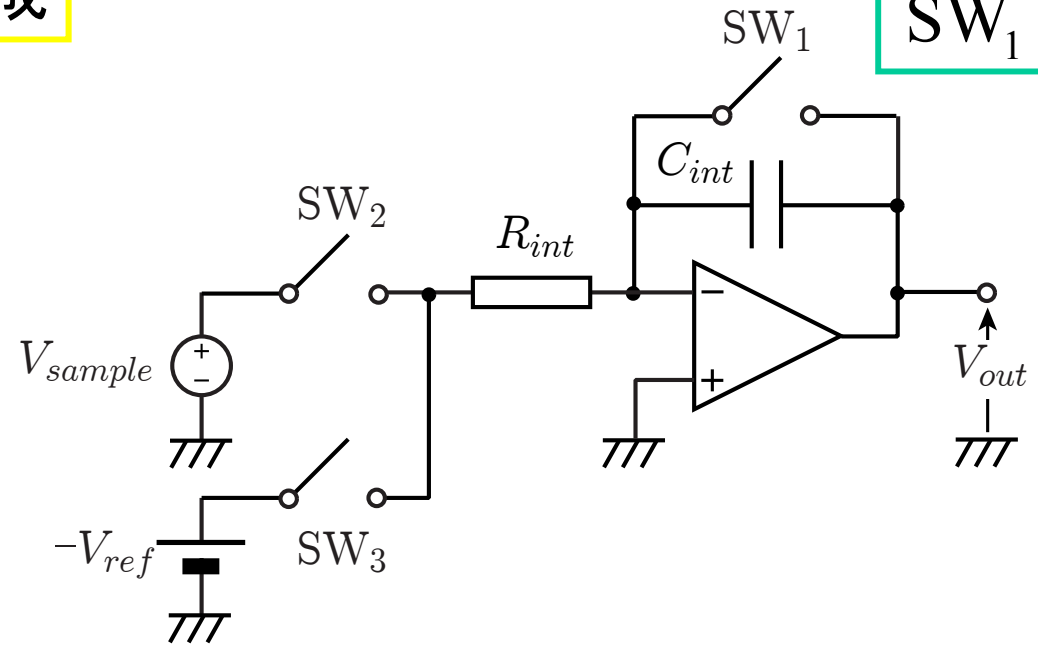




補助A-D変換器

高速性とコンパクトさ

積分型構成

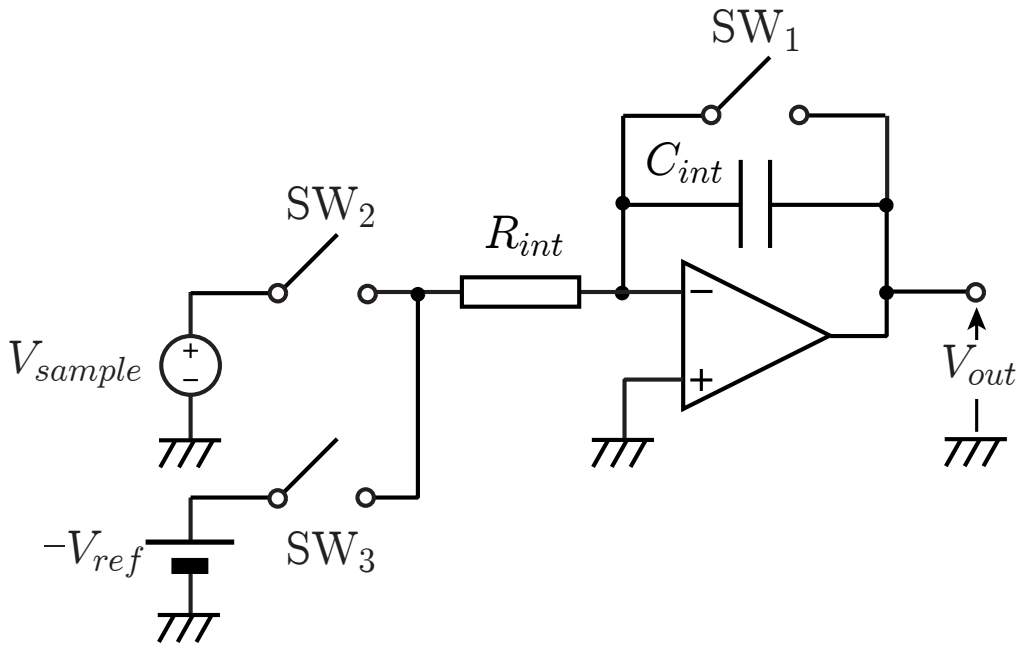


SW1 : リセット

SW2 : サンプリング

$$V_{out} = -\int_0^{T_{conv}} \frac{1}{C_{int}} \cdot \frac{V_{sample}}{R_{int}} dt$$

$$= -\frac{T_{conv} V_{sample}}{C_{int} R_{int}}$$



SW$_3$: 放電&計測

$$V_{out} = -\frac{T_{conv} V_{sample}}{C_{int} R_{int}} - \int_{T_{conv}}^{t} \frac{1}{C_{int}} \cdot \frac{-V_{ref}}{R_{int}} dt$$

$$= -\frac{T_{conv} V_{sample}}{C_{int} R_{int}} + \frac{V_{ref}}{C_{int} R_{int}} t$$

$$V_{out}=-\frac{T_{conv}V_{sample}}{C_{int}R_{int}}+\frac{V_{ref}}{C_{int}R_{int}}t_{crit}=0$$

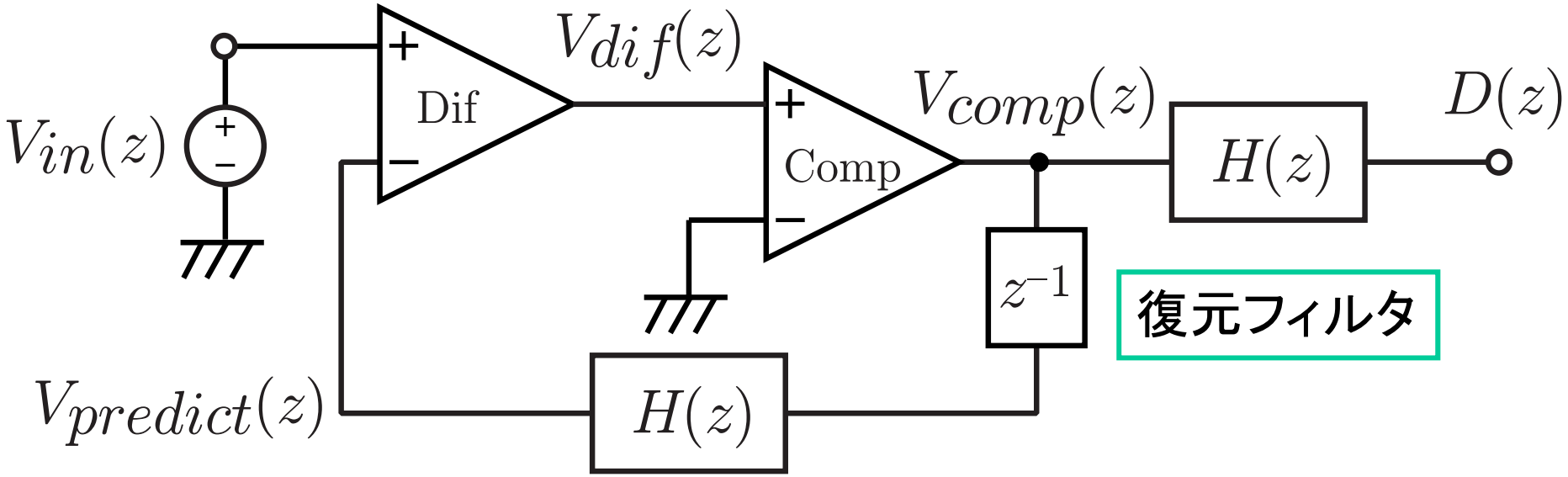
コンパレータの出力反転により検知

$$V_{sample}=\frac{t_{crit}}{T_{conv}}V_{ref}$$

精度＝時間測定の正確さ → 高精度

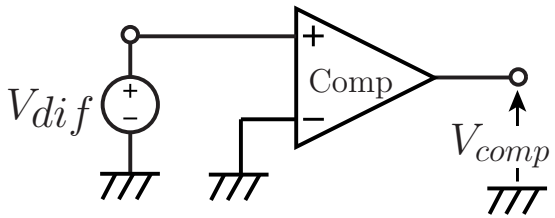
Δ-Σ変調型構成

Δ変調型構成

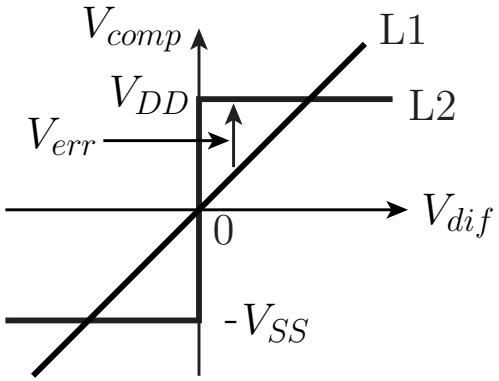


$V_{dif}(z)=V_{in}(z)-V_{predict}(z)$　により次の$V_{in}(z)$を予測

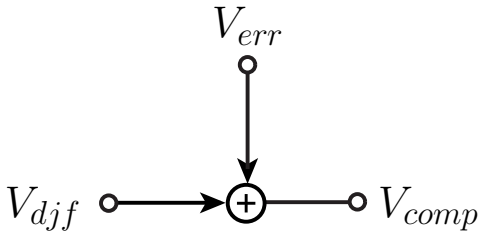
比較器のモデリング



(a)

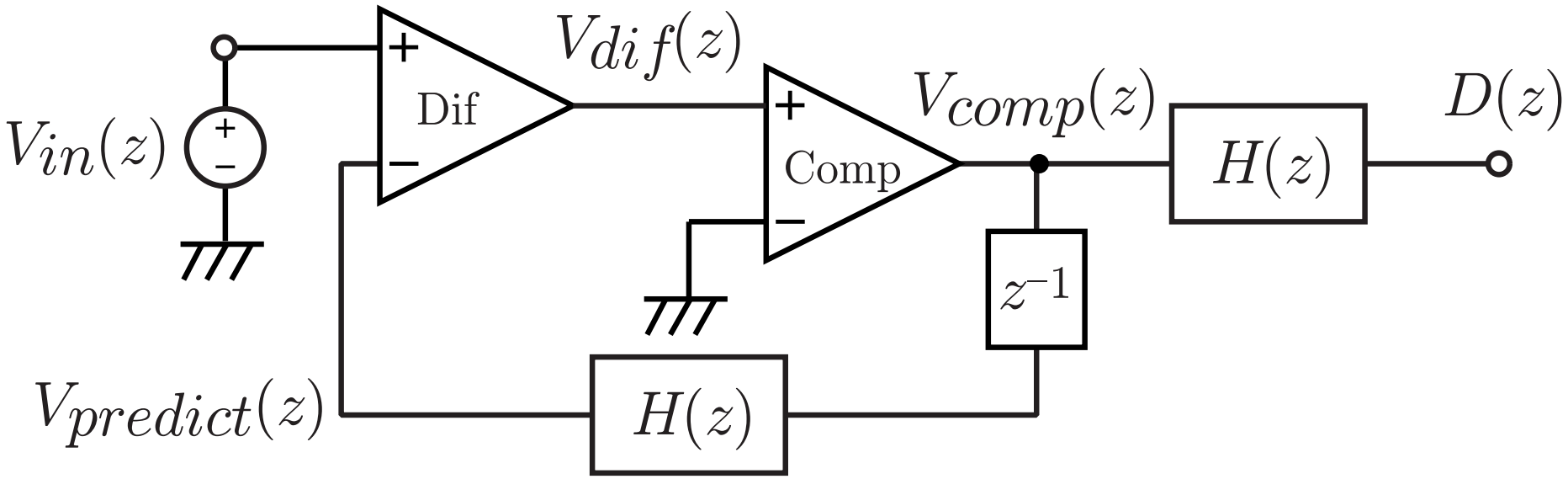


(b)



(c)

コンパレータ：非線形素子→線形素子＋雑音

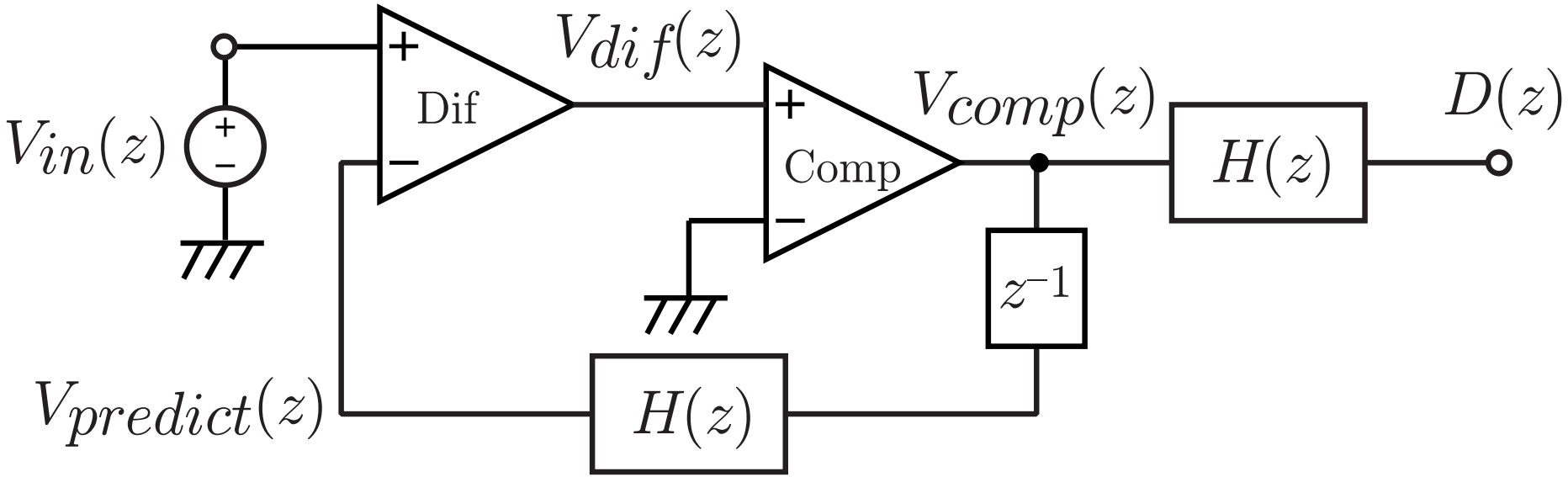


$$V_{comp}(z) = V_{dif}(z) + V_{err}(z)$$

$$= V_{in}(z) - V_{predict}(z) + V_{err}(z)$$

$$= V_{in}(z) - z^{-1}H(z)V_{comp}(z) + V_{err}(z)$$

$$\boxed{V_{comp}(z) = \frac{V_{in}(z) + V_{err}(z)}{1 + z^{-1}H(z)}}$$



$$V_{comp}(z)=\frac{V_{in}(z)+V_{err}(z)}{1+z^{-1}H(z)}$$

$$H(z)=\frac{1}{1-z^{-1}}$$

$$D(z)=H(z)V_{comp}(z)$$

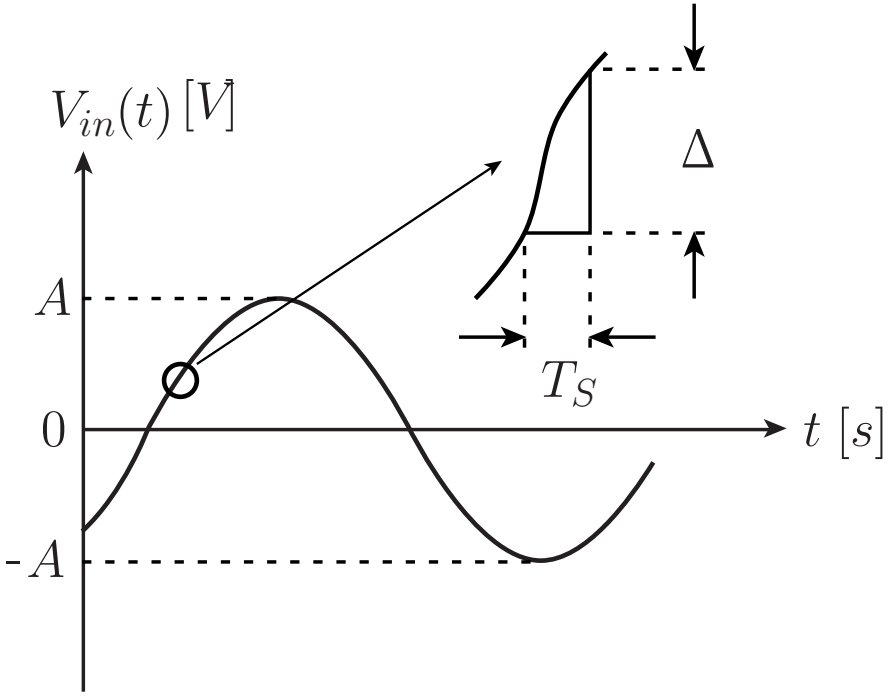
$$=\frac{1}{1-z^{-1}}\cdot\frac{V_{in}(z)+V_{err}(z)}{1+z^{-1}\frac{1}{1-z^{-1}}}$$

$$=V_{in}(z)+V_{err}(z)$$

傾斜負荷

$$V_{in}(t)=A\sin(2\pi f_{max}t+\theta)$$

f_{max}:最大信号周波数

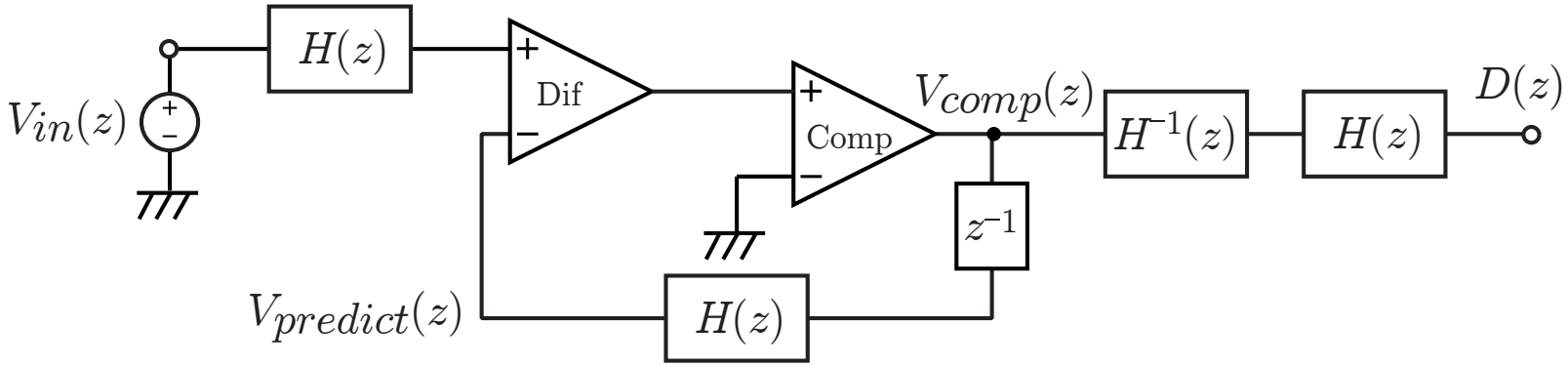


Δ:比較器の出力変化幅

T_s:サンプリング間隔

$$\max\left[\frac{dV_{in}(t)}{dt}\right]=\left.\frac{dV_{in}(t)}{dt}\right|_{V_{in}(t)=0}=2\pi f_{max}A\le\frac{\Delta}{T_s}$$

Δ-Σ変調型構成の原理



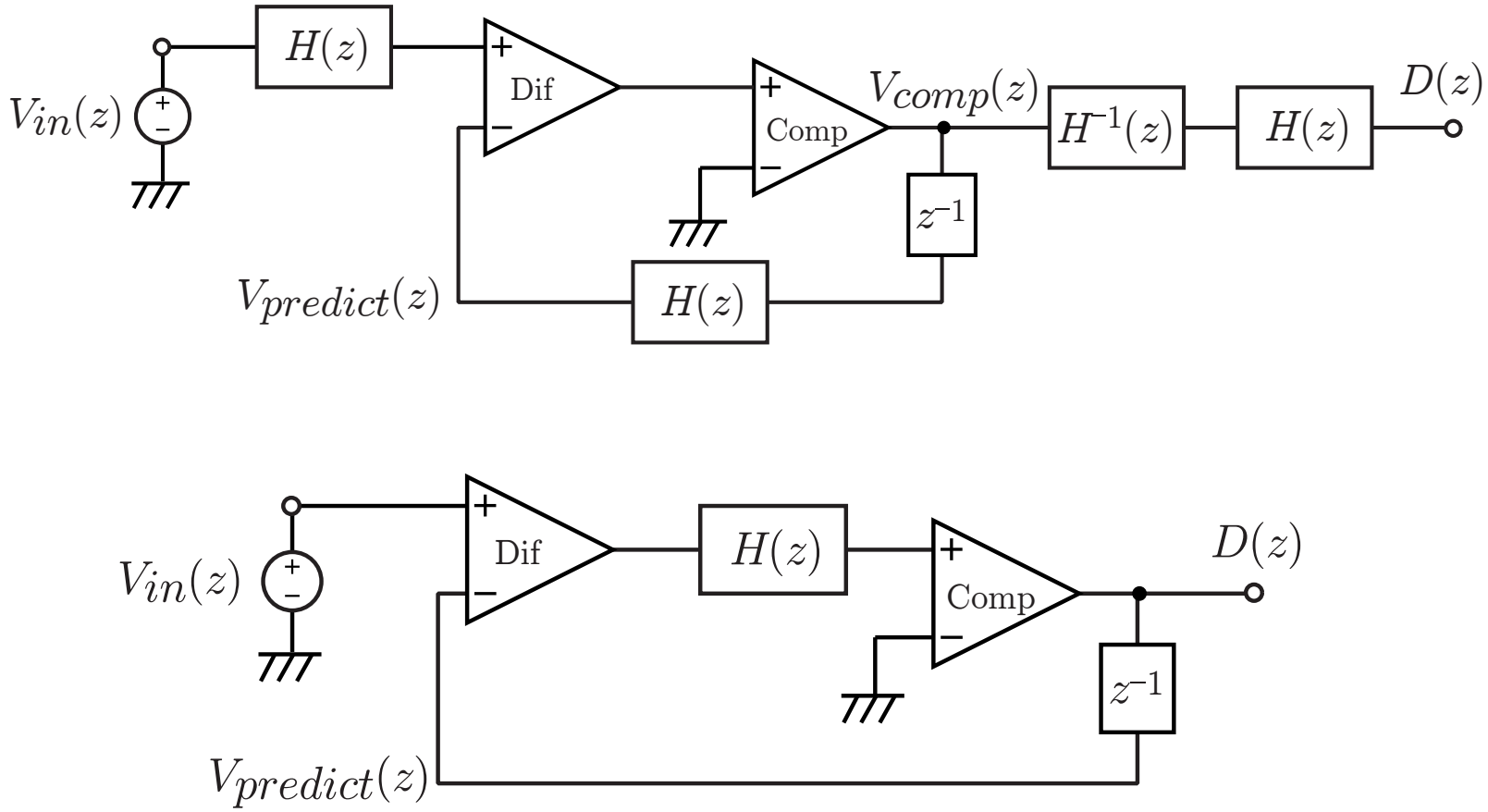
$$V_{in}(t)=A\sin(2\pi f_{max}t+\theta)$$

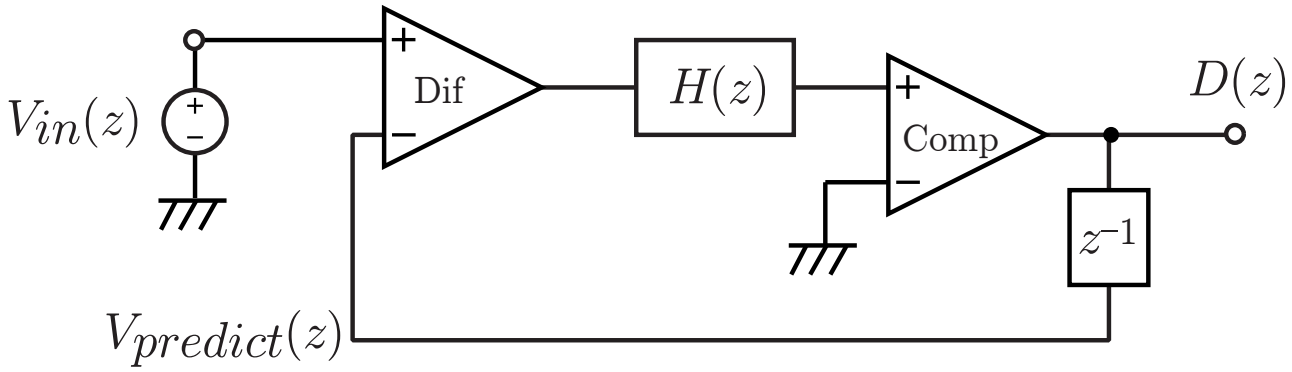
$H(z)$：積分回路

$$V_{out}(t)=\frac{-A}{2\pi f_{max}}\cos(2\pi f_{max}t+\theta)$$

最大傾斜 $:\max\left[\frac{dV_{out}(t)}{dt}\right]=A$

Δ-Σ変調型構成の簡略化



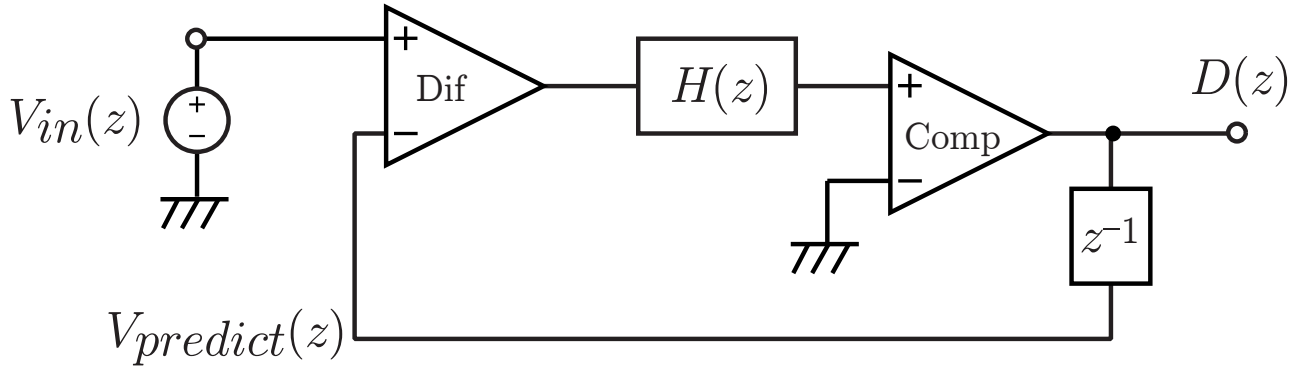


$$D(z) = V_{comp}(z)$$

$$= H(z)\{V_{in}(z) - V_{predict}(z)\} + V_{err}(z)$$

$$= H(z)V_{in}(z) - z^{-1}H(z)D(z) + V_{err}(z)$$

$$D(z) = \frac{H(z)V_{in}(z) + V_{err}(z)}{1 + z^{-1}H(z)}$$



Δ-Σ変調

$$D(z)=\frac{H(z)V_{in}(z)+V_{err}(z)}{1+z^{-1}H(z)}$$

$\longleftrightarrow$

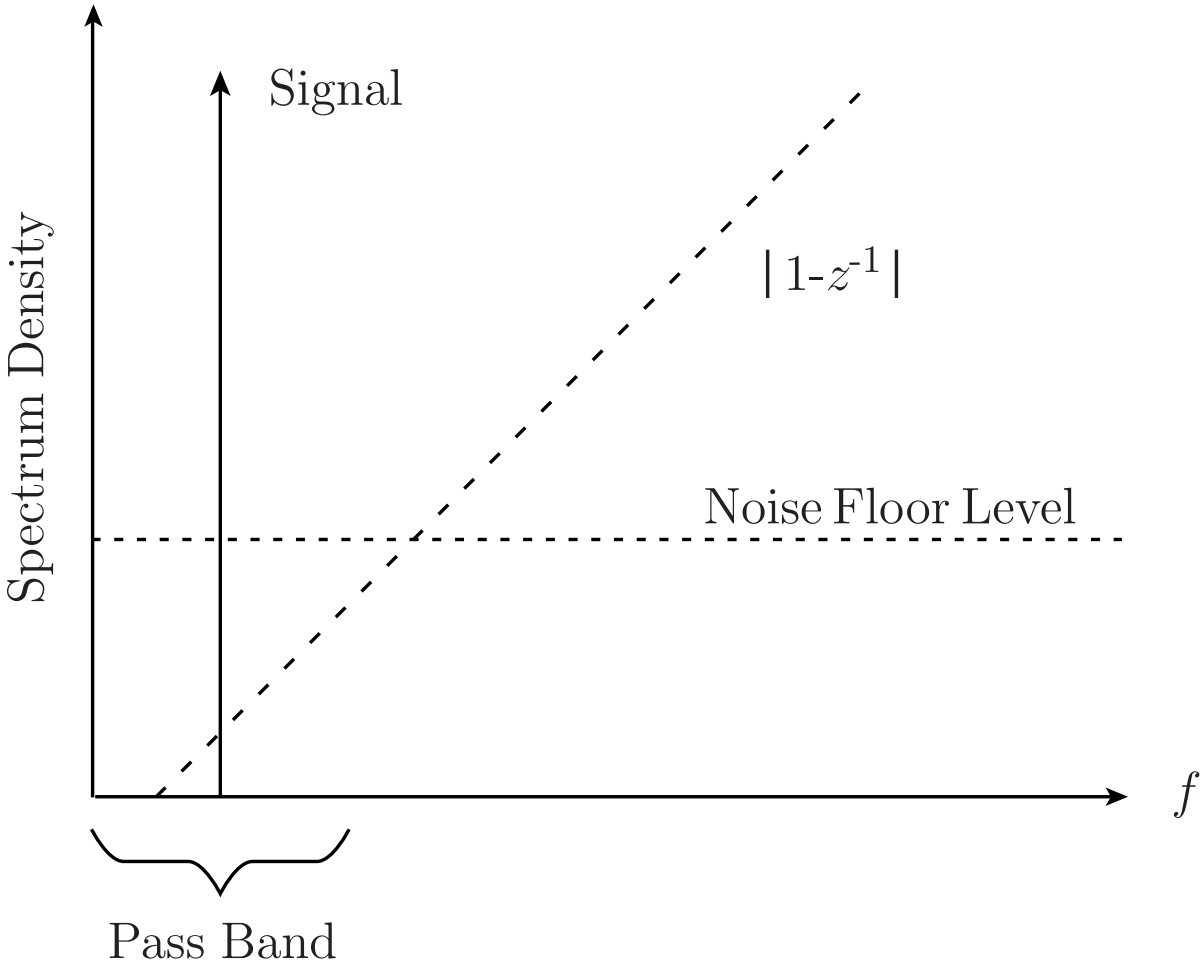
Δ変調

$$D(z)=H(z)\frac{V_{in}(z)+V_{err}(z)}{1+z^{-1}H(z)}$$

$$H(z)=\frac{1}{1-z^{-1}}$$

$$D(z)=\frac{\frac{1}{1-z^{-1}}V_{in}(z)+V_{err}(z)}{1+z^{-1}\frac{1}{1-z^{-1}}}=V_{in}(z)+(1-z^{-1})V_{err}(z)$$

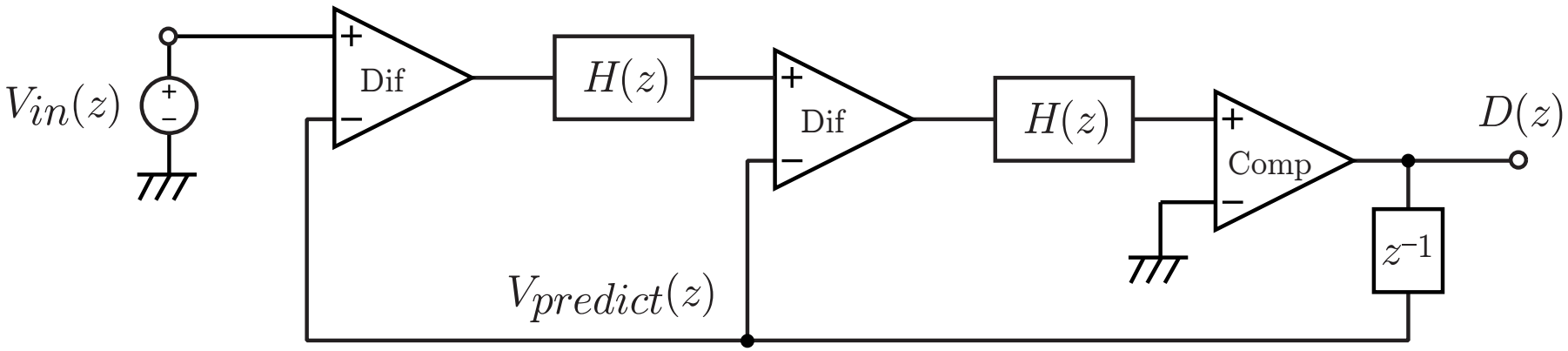
$$D(z) = V_{in}(z) + (1 - z^{-1})V_{err}(z)$$



帯域内雑音の低減

高次Δ-Σ変調型構成

高次＝不安定!?



$$D(z)=\frac{H^2(z)V_{in}(z)+V_{err}(z)}{1+z^{-1}H(z)+z^{-1}H^2(z)}$$

$$H(z)=\frac{1}{1-z^{-1}}$$

$$D(z)=V_{in}(z)+(1-z^{-1})^2V_{err}(z)$$