Outline

- Mobility Degradation in UTB MOSFETs (20nm> T_{SOI} > 5nm): Phonon Scattering
- Mobility Degradation in UTB MOSFETs (T_{SOI} < 5nm): δT_{SOI}-induced Scattering
- Coulomb Scattering in UTB MOSFETs
- Mobility in Double-Gate MOSFETs

Mobility Degradation in UTB MOSFETs



J.-H. Choi, EDL **16** (1995) 527. Seoul National Univ.

Mobility degradation have been observed in SOI MOSFETs with T_{SOI} of less than ~20nm.

Possible Reasons for Mobility Degradation







H. Wang, EDL 14 (1994) p117.

The crystal quality of SOI is the same as that of bulk Si.





mobility degradation.













Mobility Degradation: T_{sol} > 5nm



Mobility reduction in UTB MOSFETs with T_{SOI} of greater than 5nm is due to the increase of phonon scattering.

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Relationship between V_{th} and ∆V_{th}



V_{th} increase with a decrease in T_{SOI} is clearly observed in <u>both n- and p-</u> <u>MOSFET cases</u>.

V_{th} increase is due to quantummechanical effects.

Relationship between ∆V_{th} and T_{SOL}





Hole Mobility as a function of T_{sol}



Hole mobility decreases monotonically as T_{SOI} decreases, which is attributable to the increase of phonon scattering in inversion layer.



Electron Mobility as a function of T_{SOI}



Theoretical vs. Experimental



Why mobility degradation even at 25K? Why small enhancement?

In order to clarify the reason, the effect of SOI thickness on C-V and I-V characteristics are thoroughly investigated by comparing experimental data with selfconsistent-calculation data of Schrödinger and Poisson equations.



V_{th} versus T_{SOI} (nMOS)





Effect of δT_{SOI} on Mobility



$$h_n = \frac{h^2}{8m^* t_{\rm SOI}^2}$$

Potential fluctuation ΔV

$$\Delta V = \left[\frac{\partial E_n}{\partial T_{\rm SOI}}\right] \cdot \Delta = -\frac{h^2}{4m^* T_{\rm SOI}^{3}} \cdot \Delta$$

E

 δT_{SOI} -limited mobility μ_r

$$\mu_r \propto \left[\frac{1}{\Delta V}\right]^2 \propto T_{\rm SOI}^{6}$$

 δT_{sol} -limited mobility μ_r shows T_{sol}^6 dependence.



Electron Mobility as a function of T_{SOI} at T=25K T_{SOI}^{0} T_{SO



Hole Mobility at T=25K



dT_{sol}-scattering is also effective in pFETs.



Condition to Suppress δT_{sol}-induced Scattering



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Interface States generated by Fowler-Nordheim Stress

Interface States induced by Fowler-Nordheim (FN) Stress



 D_{it} can be controlled well by Q_{ini} in Bulk FETs.

µ_{Coulomb} by D_{it} in Bulk FETs

 $\mu_{\rm Coulomb} \propto {\sf N_s}^{0.5}$

 $\mu_{\rm Coulomb} \propto \Delta D_{\rm it}^{-1}$

J. Koga et al., SSDM 1994, p895.





Coulomb Scattering as a Function of T_{SOI}





Effect of *D_{it}* on FC and BC Mobility



$\mu_{\rm eff}$: Initial Characteristics



Front-channel μ_{eff} agrees well with back-channel μ_{eff} .



µ_{Coulomb}: front vs back channel Thinner (4.2nm) SOI nFETs Experimental H_{Coulomb} [cm²/Vsec] T_{SOI}=4.2nm Q_{inj} [C/cm²] BC 0.005 FC 0.015 front-channel back-channel 0 10¹² $N_{s} [cm^{-2}]$ In thinner SOI nFETs, BC mobility is almost the same as FC mobility in the entire N_s regions.



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Coulomb Scattering in Double-Gate MOSFETs

µ_{eff}: Single-Gate vs Double-Gate



In 22nm SOI nFET, double-gate (DG) μ_{eff} agrees well with single-gate (SG) μ_{eff} .





greater screening effects in DG MOSFETs.

Transport in DG FETs as a function of T_{sol}





Double-gate μ_{eff} is greater than single-gate μ_{eff} in 7.4-nm and 14.9-nm MOSFETs, which can be attributed to volume inversion.



Why smaller μ_{eff} in DG FETs?



resulting the higher occupancy in 4-fold valleys.

Valley Occupancy: SG vs DG



- The occupancy of 4-fold valley is higher in DG than in SG.
- δT_{SOI}-induced scattering is 670 times stronger in 4-fold valley than in 2-fold valley.

$$\mu_{\delta ext{Tsoi}} \propto \left(rac{m_c}{m_z}
ight)^2$$

 m_c : conductivity mass m_z : vertical mass

In UTB MOSFETs, δT_{SOI} -induced scattering is severe in DG than in SG, which results in smaller μ_{eff} in DG at higher N_s .

5-atomic-layer MOSFETs

5-atomic-layer MOSFET Cross-sectional TEM of MOSFET Channel

Gate Oxide 10nm

Buried Oxide



5-atomic-layer (0.7-nm) MOSFETs are successfully fabricated.



 $C_{gc,max}$ of sub-1-nm MOSFE is is almost the same as $C_{gc,max}$ of 15-nm MOSFETs, suggesting that there is no void in sub-1-nm film.



thinner sub-1-nm MOSFETs are observed.



Summary (I)

 Electron mobility enhancement with a decrease in T_{SOI} is demonstrated, for the first time

 SOI-thickness-flucutation-induced scattering is observed and evaluated, for the first time.

In order to enjoy the full advantages of UTB MOSFETs, atomically flat SOI film should be realized in deep-sub-20nm regime.

Summary (II) µ_{Coulomb} in UTB MOSFETs

- μ_{Coulomb} is less in thinner body MOSFETs
- Back D_{it} is less effective to μ_{eff} degradation than front D_{it} . However, at lower N_s , the effect of Back D_{it} is comparable to that of Front D_{it} .
- Effect of Back D_{it} is almost that same as that of Front Dit in UTB MOSFETs.
- μ_{Coulomb} in DG is greater than μ_{Coulomb} in SG.
- **Transport in Double-Gate MOSFETs**
 - The lowering of μ_{eff} in DG, compared to SG, is observed, which is attributable to δT_{SOI} -induced scattering.

Sub-1-nm MOSFETs

• The operation of sub-1-nm MOSFETs is confirmed, for the first time.

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