RF Devices and RF Circuit Design for Digital Communication

Agenda

- Fundamentals of RF Circuits
- Transmission Line
- Reflection Coefficient & Smith Chart
- Impedance Matching
- S-matrix Representation
- Amplifiers & Unilateral Gain
- RF Devices
- Digital RF

- Fundamentals of RF Circuits
  - Lumped-element circuits: $\lambda \gg L$, L is a typical length of device.

    e.g. $\lambda = 30$ cm for $f = 1$GHz
  - Distributed-element circuits: $\lambda \sim L$

    Lead Line becomes a coil and/or capacitance.

Historically **Rayleigh** analyzed an undersea cable based on distributed circuit concept.

→**Image Impedance and Propagation Constant**

– Basic distributed element: **Transmission Line**

F-matrix of Transmission Line

$$F = \begin{bmatrix} \cos\theta & jZ_0 \sin\theta \\ j\sin\theta / Z_0 & \cos\theta \end{bmatrix}$$

Z_0 : Characteristic impedance of Transmission Line

θ : Phase delay $\left(= \beta\ell = \omega\sqrt{\varepsilon\mu}\,\ell = \omega\ell / v\right)$

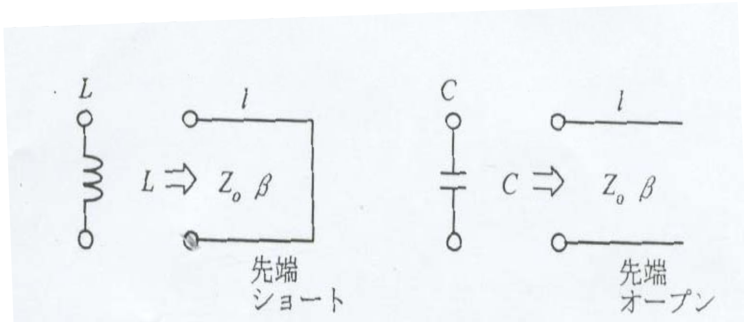
ℓ : length

v : velocity

Transmission Line

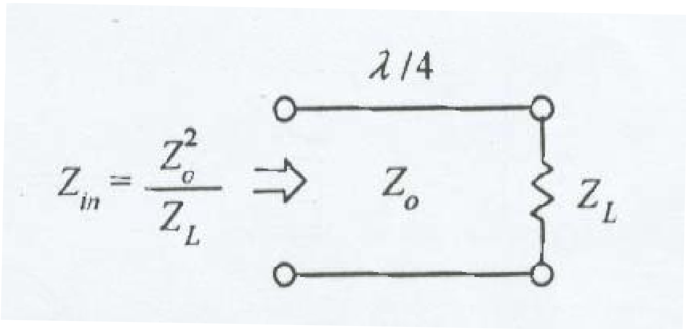
⇩

Inductance, Capacitance,
Filter, Impedance Transformer

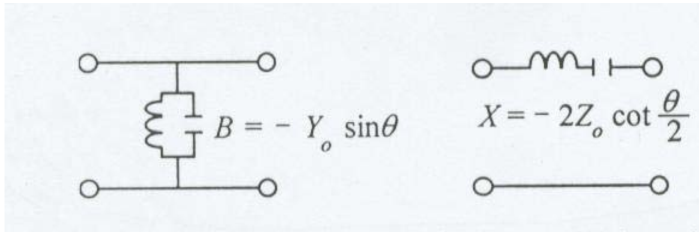


Short-end Open-end

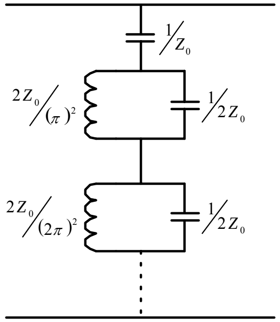
Impedance Inverter : ZL ⇒ Zin



Shunt to Series Connection



Equivalent Circuit of Transmission Line by Foster Expansion

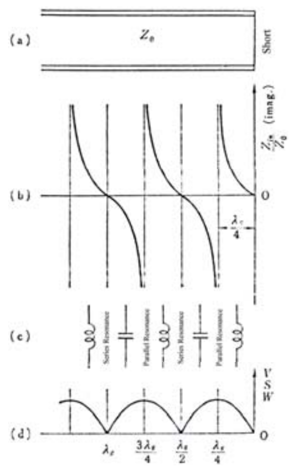


A Series Connection of Parallel Resonance Circuits

– Short (Open) - circuited load: → Reactance element
$X_{in} = Z_0 \tan\theta$: short-circuited load

$$\boxed{\begin{array}{l} 0 < \theta < \pi/2 \ : \text{Inductance} \\ \quad \theta \approx \pi/2 : \text{Parallel resonance circuit} \\ \pi/2 < \theta < \pi : \text{Capacitance} \end{array}}$$

– Stub
– Quater-wavelength Transformer
→ Matching coating lense



Short-terminated Line

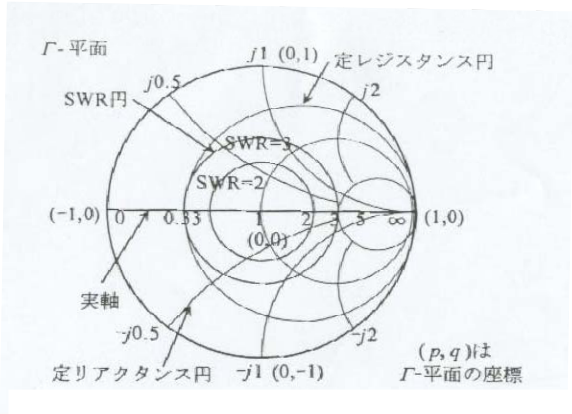
- Reflection coefficient (Γ) and Load Impedance (Z_L)

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} : \text{Bilinear mapping}$$

Z_0: reference characteristic impedance

Circle to Circle Mapping
(Moebius Transform)

Smith Chart



$$
\begin{aligned}
&\mathrm{Re}(Z_L) > 0 : |\Gamma| < 1 \ \text{(Passive)} \\
&\mathrm{Re}(Z_L) = 0 : |\Gamma| = 1 \ \text{(Lossless)} \\
&\qquad\qquad \text{Reflection type phase modulator} \\
&\mathrm{Re}(Z_L) < 0 : |\Gamma| > 1 \ \text{(Active)} \\
&\qquad\qquad \text{Reflection type amplifier}
\end{aligned}
$$

- Voltage Standing Wave Ratio (VSWR)≥1

$$\mathrm{VSWR} = \frac{V_{\max}}{V_{\min}} = \frac{V_i + V_r}{V_i - V_r}$$

$$|\Gamma| = \frac{V_r}{V_i} = \frac{\mathrm{VSWR}-1}{\mathrm{VSWR}+1}$$

V_i : incident wave

V_r : reflected wave

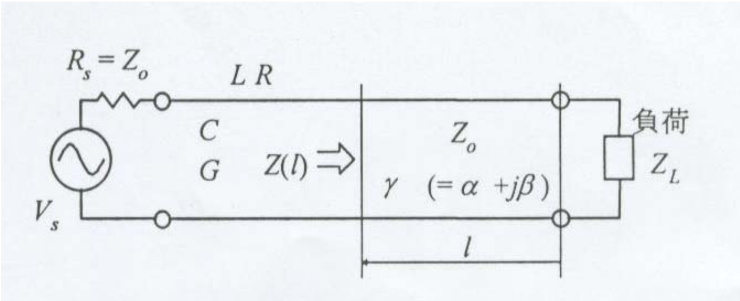
- Special Terminations / Circuits
  – Matched load: ($Z_L = Z_0$) →Γ= 0, No reflection

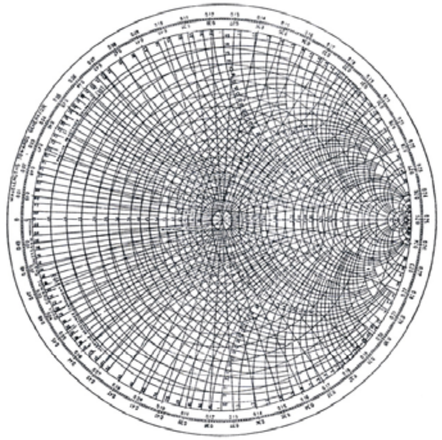
– **Smith-chart and its usage**
- Smith-chart (Bell Lab. 1950's)

$$Z_{\mathrm{in}} = Z_0 \frac{Z_L + jZ_0 \tan\theta}{Z_0 + jZ_L \tan\theta}$$

$$
\boxed{
\begin{aligned}
&Z_L \to \tilde{Z}_L = \frac{Z_L}{Z_0} \to \Gamma_L = \frac{\tilde{Z}_L - 1}{\tilde{Z}_L + 1} \to \\
&\Gamma_{\mathrm{in}} = \Gamma_L \exp^{-j2\theta} \to \tilde{Z}_{\mathrm{in}} = \frac{1+\Gamma_{\mathrm{in}}}{1-\Gamma_{\mathrm{in}}} \to Z_{\mathrm{in}}
\end{aligned}
}
$$

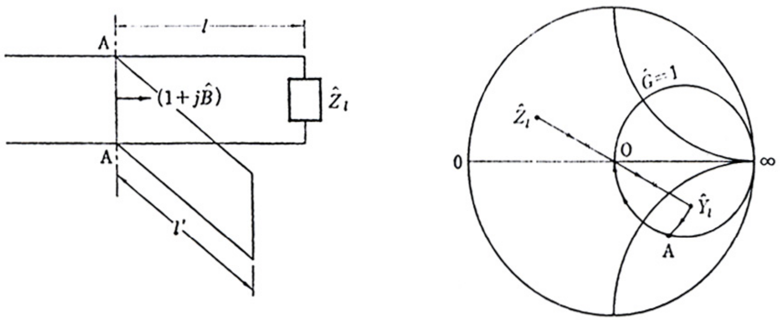
Impedance Transforming





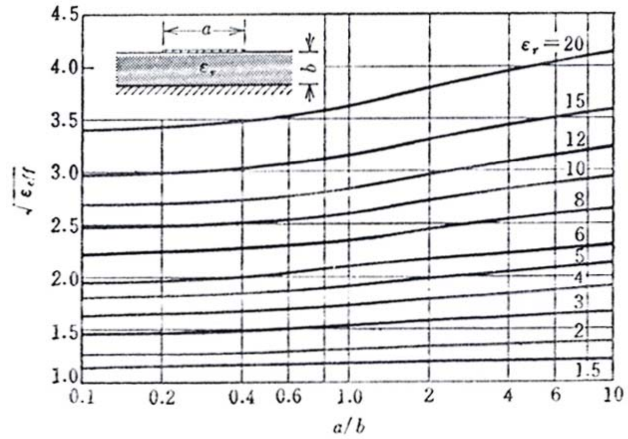
Smith Chart

- How to use Smith-chart
  - Matching Circuit Design



Single-stub Matching

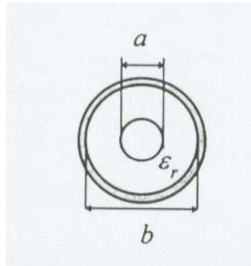
- Microstrip Line
  - Effective permittivity and guided wavelength
  - Characteristic Impedance
  - Several notes : Finite conductor thickness



Microstrip Line (Effective Permittivity)

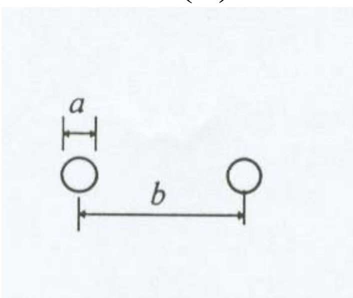
Coaxial Line

$$Z_0 = \frac{138}{\sqrt{\varepsilon_r}} \log b/a$$

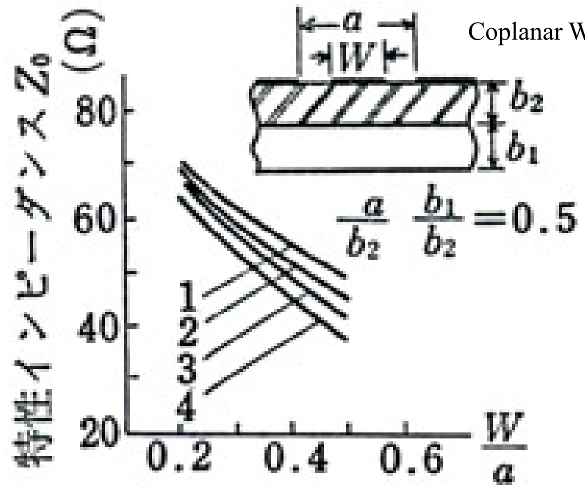


Pair-cable Line

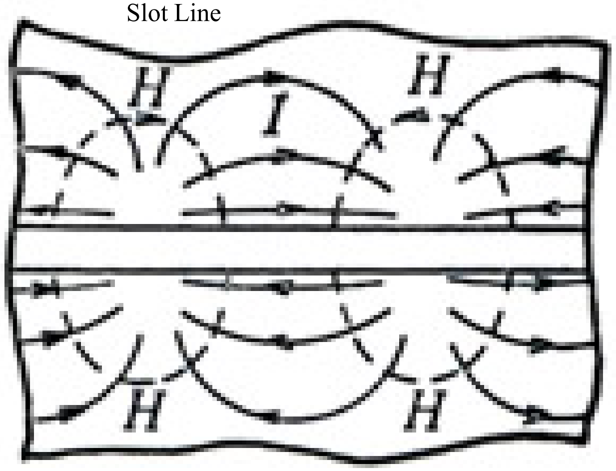
$$Z_0 = 120 \cosh^{-1}\left(\frac{b}{a}\right)$$



Coplanar Waveguide

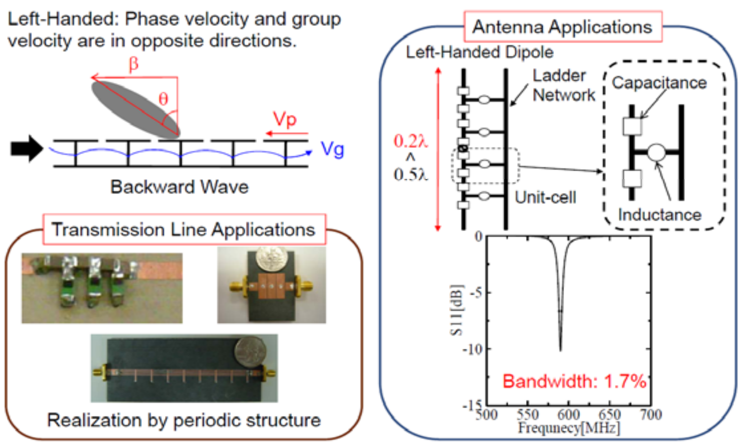


Slot Line

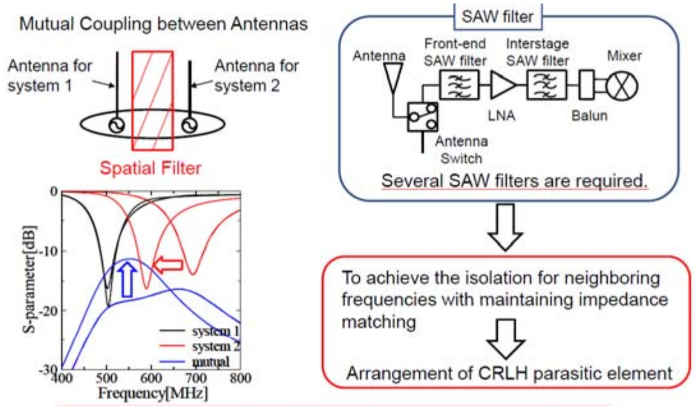


Meta Material

- Right-Hand Transmission Line
- Left-Hand Transmission Line
- Composite RH/LH Transmission Line
- Compact Directional Coupler
- Super-Lense

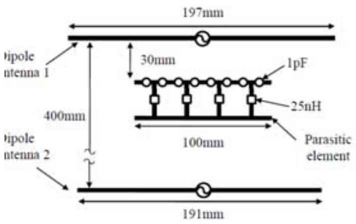


Left-Handed Metamaterial: Miniaturization, but Narrow Bandwidth

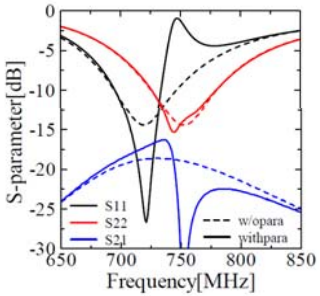


Mutual coupling reduction between two dipole antennas using CRLH parasitic elements are clarified.

Mutual Coupling Reduction Using CRLH Parasitic Element 11



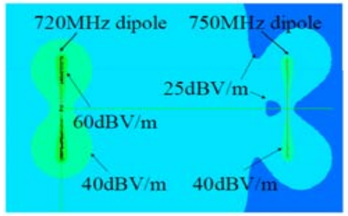
Configuration of two dipole antennas with CRLH parasitic element



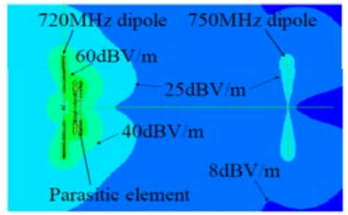
S-parameter characteristics

When CRLH parasitic element is used, the value of S21 decreases sharply at around 750 MHz due to band rejection frequency of CRLH parasitic element.

Near Field Distributions at 750 MHz 1



Without parasitic element



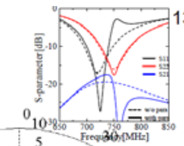
With parasitic element

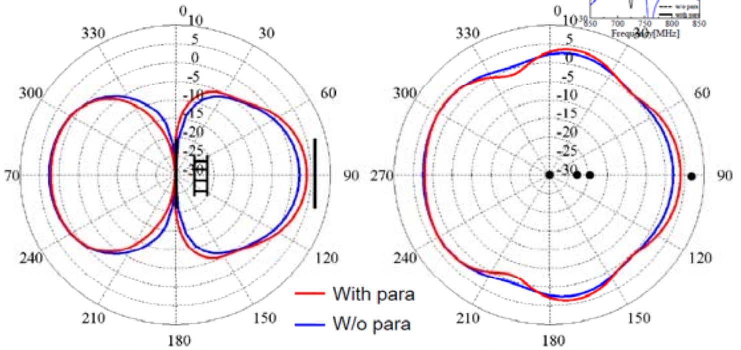
Electric field distribution spreads from 720 MHz dipole to 750 MHz dipole without parasitic element.

Electric filed distribution concentrates around 720MHz dipole with parasitic element.

Radiation Patterns at 720 MHz

13





Vertical Plane

Horizontal Plane

Little effect due to arrangement of parasitic element

Radiation Patterns at 750 MHz

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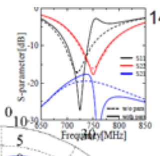
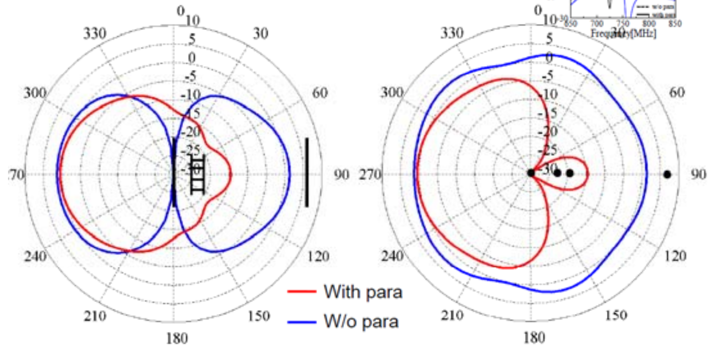




Vertical Plane

Horizontal Plane

Radiation reduces in direction to parasitic element.

- **S-parameter and RF Circuit Design**
  - S-parameter (1950's ← Nuclear Physics)

$$\text{voltage, current} \rightarrow \text{incident wave, reflected wave}$$
$$\text{impedance} \rightarrow \text{reflection coefficient}$$
$$\text{impedance matrix} \rightarrow \text{scattering matrix}, [S]$$

For lossless circuit, **S-matrix** = **Unitary Matrix**

For lossy circuit, $S^{\dagger}S \leq I$ Para-unitary

For Reciprocal circuit, S-matrix = Symmetric matrix

SVD (Singular Value Decomposition)

$S = U^{\dagger}DV$ (Youla)

U,V : Unitary matrix (Lossless Circuit)

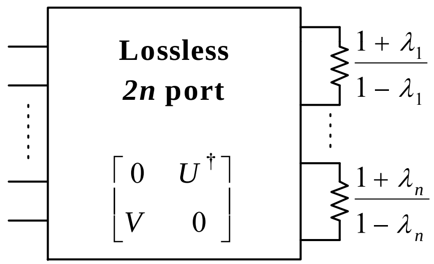
D: Diagonal Matrix (→ Isolated *n*-port circuit)

$$D = \mathrm{Diag}[\lambda_1, \ldots, \lambda_n]$$

$\lambda_i < 1$ → resistance

$\lambda_i > 1$ → negative resistance

Generalization of Darlington realization



– Basics of RF Circuit Design

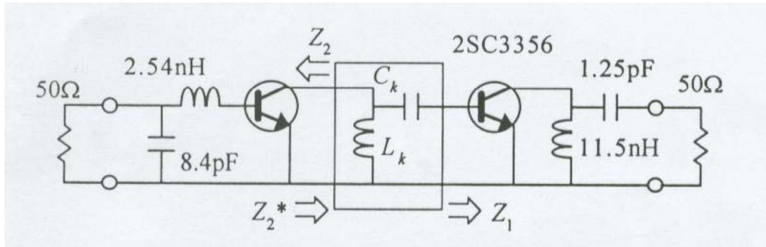
- Impedance Matching Circuits

$$Z_g = Z_L^{\ *}$$

Z_g : Generator Impedance

Z_L : Load Impedance

Conjugate Matching



Unilateral Transducer Gain G_{TU}

(For the case, $S_{12} = 0$ Reverse transfer coefficient from output to input)

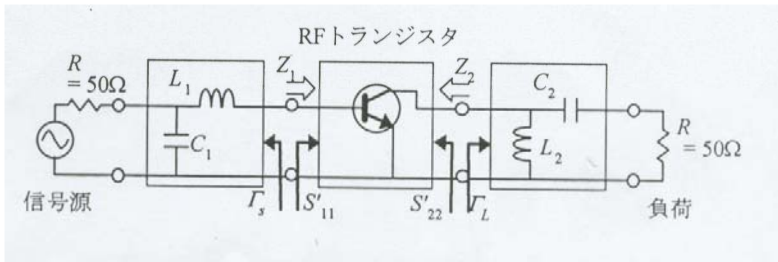
$$\text{FET } S\text{-parameter} \begin{vmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{vmatrix}$$

$$G_{TU} = \frac{\left(1-|\Gamma_s|^2\right)}{|1-S_{11}\Gamma_s|^2} \cdot |S_{21}|^2 \cdot \frac{\left(1-|\Gamma_L|^2\right)}{|1-S_{22}\Gamma_L|^2}$$

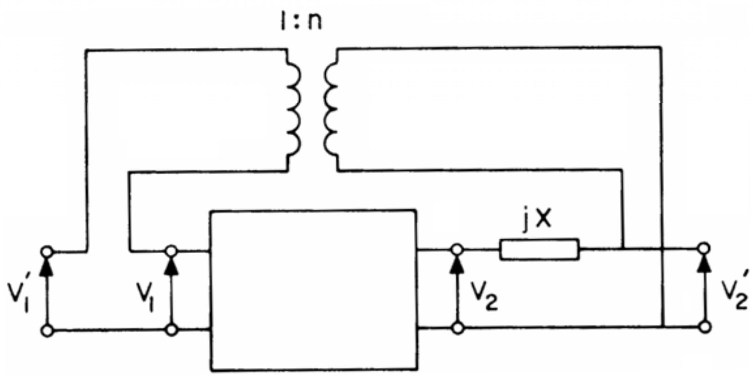
$$= G_s \cdot G_0 \cdot G_L$$

$$G_{TU,\max} = \frac{1}{1-|S_{11}|^2} \cdot |S_{21}|^2 \cdot \frac{1}{1-|S_{22}|^2}$$

Input and Output Matching Circuit



Unilateral Gain U : Mason's Invariant



Unilateralization of a two-port network

Circuit Invariant

- Unilateral Gain (U)
- Maximum Available Gain (MAG)
- Noise Measure (M)
- 2-state diode （m、Q)
- Circulator Invariant (α)
- Directional Coupler Invariant （K)

2-state device

- On-state impedance Z1 , Off-state impedance Z2
- M=|Z1-Z2|/|Z1+Z2*| ⇒ Invariant w.r.t. Lossless 2port connection
- M=|Γ1-Γ2｜/｜1－Γ1Γ2*｜⇒ Optimum BPSK Direct Modulation Design

- **RF Devices**
  - Passive Components / Circuits
    - Reactance Elements
      - Distributed-element:
        Open-stub, Short-stub, Line Gap
        Wide Line, Narrow Line
      - Lumped-element:
        Spiral Inductor, Gap Capacitor, Thin Film Capacitor

Attenuators:

Thin Film Resistor

- Impedance Transformers:

  Quarter-wavelength Impedance Transformer

$$Z_{\text{in}} = \frac{Z_0^{\;2}}{Z_L}$$

- Resonator:
  - Lumped Element Type
  - Microstrip Line Type
  - Dielectric Resonator Type (Good Ceramic)

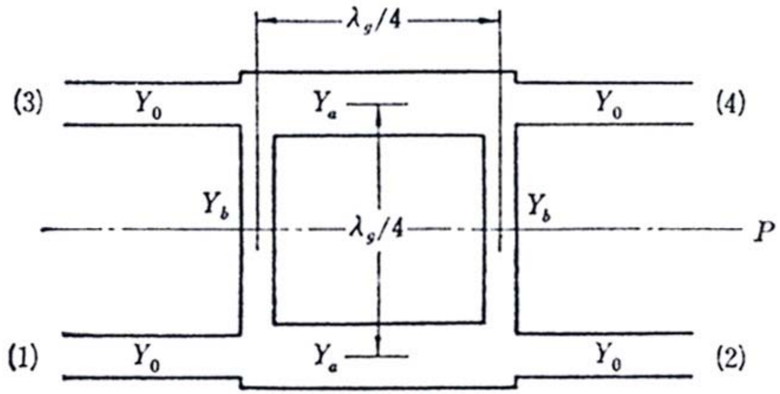
– Distributing Components / Circuits

- Directional Coupler:

  Power Monitor, Balanced Type Modulator / Amplifier / Mixer

  Lossless reciprocal matched two-fold symmetry 4-port

  → Perfect Directional Coupler with 90deg. Phase Difference
  - Coupled Line Type
  - Inter-digital Type
  - Branch Line Type
  - Rat-race Type



Branch-line Coupler

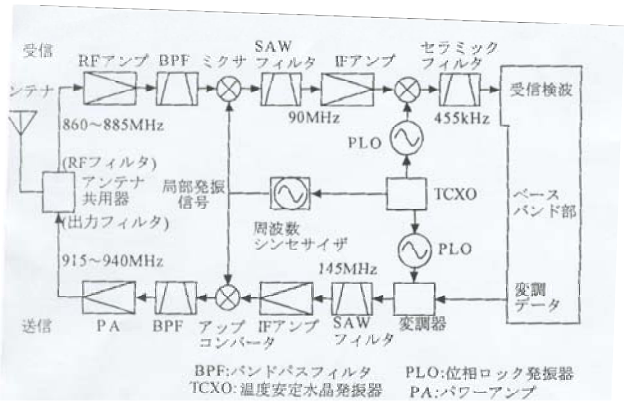
- Power Divider / Combiner:

  Perfect Matching + Perfect Isolation → Absorbing Resistance
- Filter
  - Low Pass Filter (LPF):
    L, C Ladder Filter
  - Band Pass Filter (BPF):
    Half-wavelength transmission line resonator
  - Band Stop Filter (BSF):

- **Transmission Scheme and RF Circuits**

Objectives: Low Power Consumption, Higher Frequency, Small Size, Low Weight

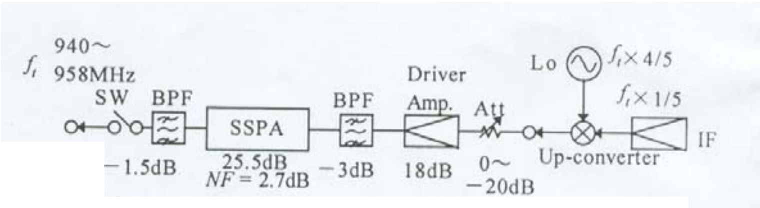
Block diagram of Transceiver



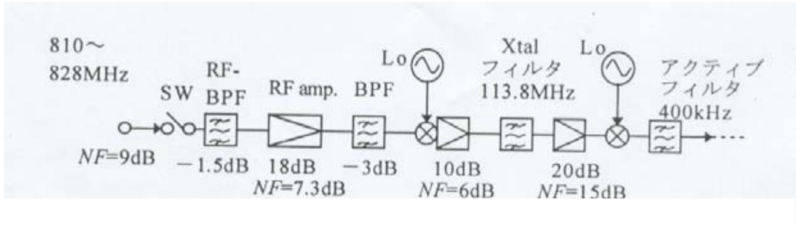
– Basic configuration of RF Circuits: Super-Heterodyne

Mixer: Up-conversion Down-conversion Amplifier: Power Amp. (TX) Low Noise Amp. (RX) Oscillator: Local Oscillator Filter: LPF, BPF

TX Level Diagram



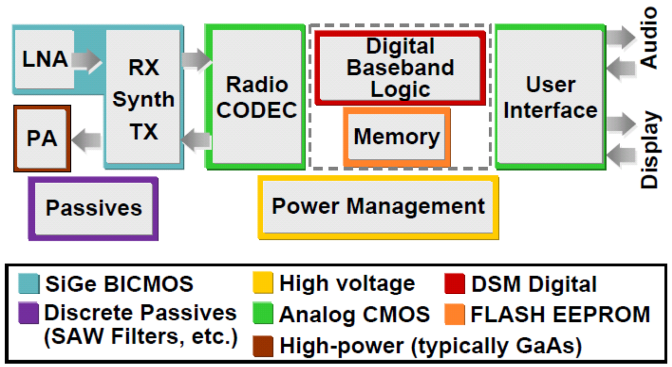
RX Level Diagram



Digital RF Circuits

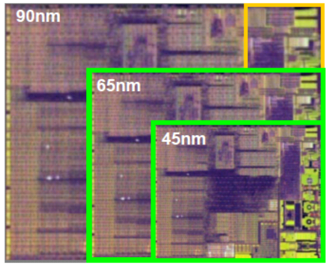
- RF-CMOS Technology
- Analog Signal Processing & Digital Signal Processing
- Continuous Time & Discrete Time
- Direct Conversion & Sampling
- Built-in RF Self Test & Calibration

Typical Cell-Phone Block Diagram



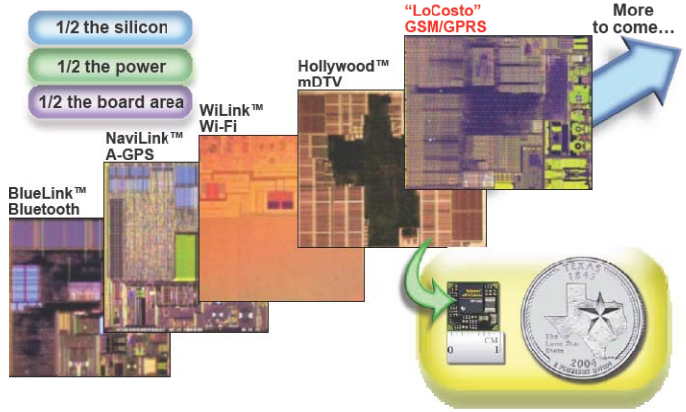
Area and cost must be reduced → integrate ！

SoC Drives Cost Reduction

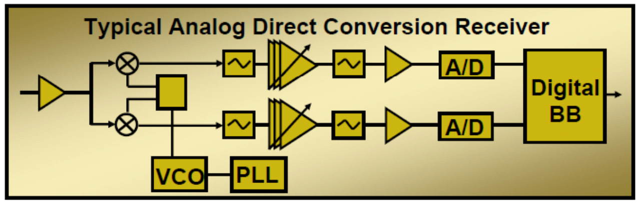


- SoC Integration Includes:
  - Digital baseband
  - SRAM
  - Power management
  - Analog
  - RF
  - Processors & Software
- The DRP technology enables digital implementation of traditional analog RF functions in standard CMOS
- Most advanced process technology used to maximize integration while minimizing cost
  - 90nm (shipping)
  - 65nm (mature design)
  - 45nm and beyond (preliminary)

DRP/SoC Proven Across Many Products

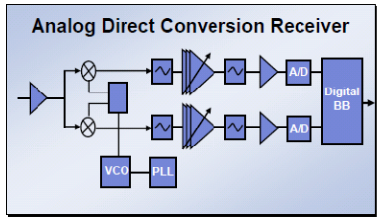


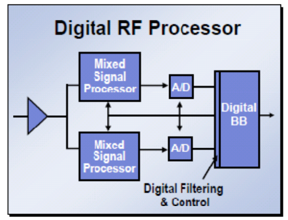
Analog RF Challenges in DSM CMOS



- Power supply voltage overhead – must scale to ~1Volt
- Passives – need high quality inductors, caps, etc.
- Noise/clock coupling – time-align to avoid interference
- Development time – should not delay node migration of digital baseband processor portion.
- Cost – need to minimize multiple pass testing and yield loss

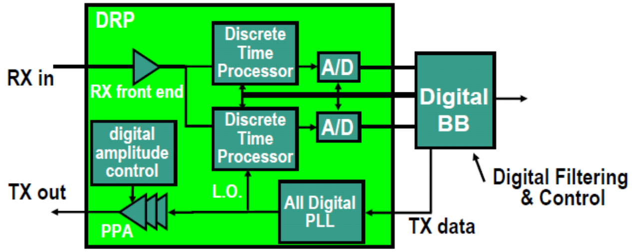
Digital Transceiver Architecture





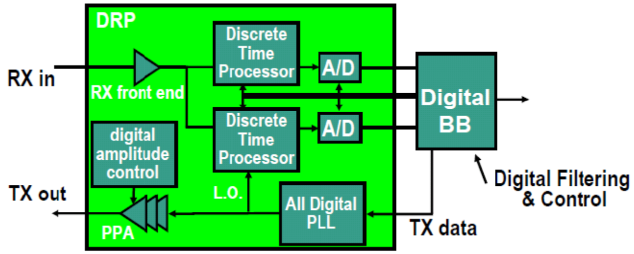
Conventional Direct Conversion is a Great Technology
… but not well suited for CMOS integration
… and digital techniques improve perf/power
… and digital provides a path to SDR!!

The DRP Approach for Transceivers



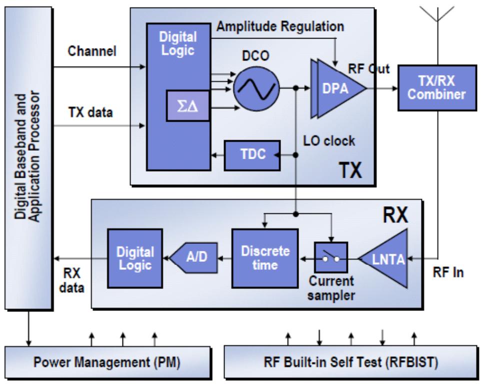
- **Minimize analog and RF circuitry**
  - Self-calibrate remaining analog (with dedicated processor)
  - Relax passive requirements as much as possible
- **Digital approach speeds debug and development**
- **Self-test and calibration made possible**
- **Production yield dominated by silicon defect density**

The DRP Approach (continued)



- **Move functions to domains of CMOS-process strengths**
  - Operate in fine time resolution, avoid fine voltage resolution
  - Inductor area could be equal to ~100K gates (use digital!)
  - Use switched cap techniques – excellent matching in DSM CMOS (not sensitive to process variations)
  - Logic and switched cap circuits can work well at low voltage

DRP RF Architecture



0.2, 1.25, 2.5,5, 10, 15, 20MHz BW

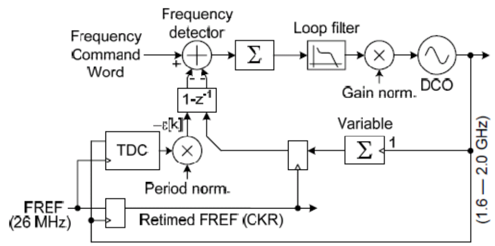
450, 800, 900, 1800, 1900, 2100, 2500, 3400MHz Transmission bands

GMSK, QPSK, 8-PSK, 16QAM, 64QAM Modulation

TDMA, FDMA, CDMA, OFDMA, IFDMA schemes

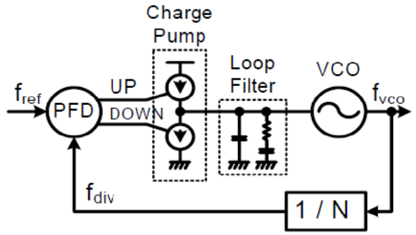
Looks almost like SDR!!

All-Digital PLL Vs. Conventional PLL



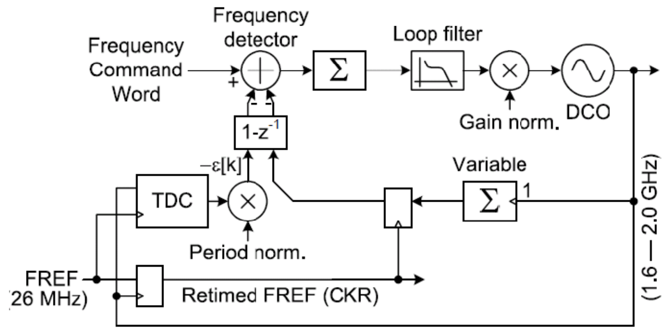
- The ADPLL is “Analog” only in FF, TDC and DCO
- Varactors operate in low sensitivity states (“on” or “off”)
- Self-calibration is easy -- DCO gain can be assessed numerically
- Can lock very fast, dynamically change loop bandwidth (<10µsec), and collect register settings for “instant restart” on frequency.

Drawbacks of Conventional Analog PLL

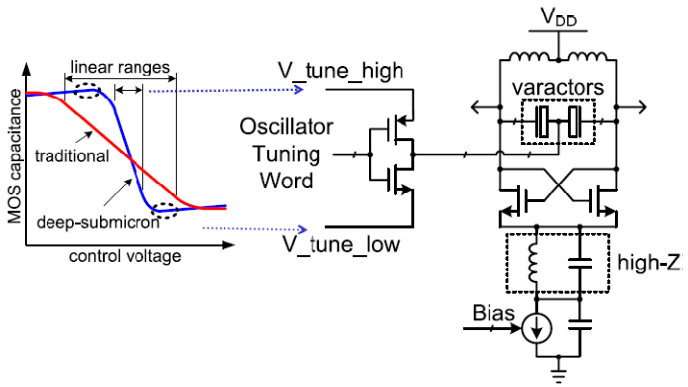


- Many analog functions = multiple noise sources
- Varactors in VCO are sensitive (high tuning factor, i.e. KVCO)
- Loop filter may be large, leaky capacitors (for open loop "freeze"), variances in passives…
- Hard to calibrate
- Lock times can be long (>100μsec)

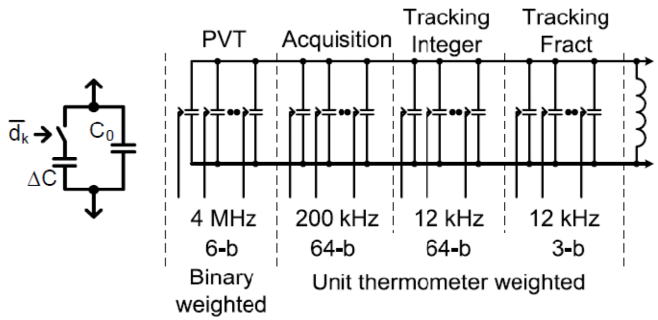
All-Digital PLL (ADPLL)



Digitally-Controlled Oscillator Core



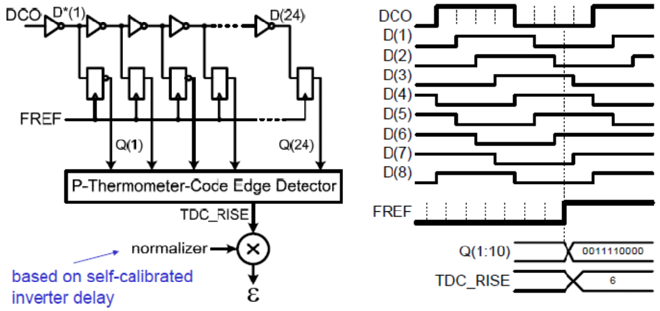
DCO Varactor Banks



High-speed dithering and dynamic element matching are used to achieve high resolution (LSB = ~1.5Hz).

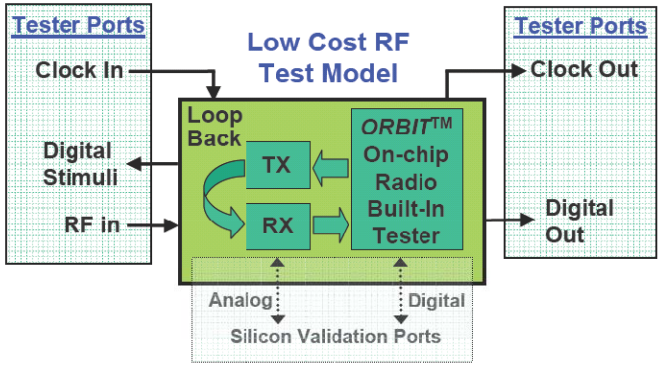
Time-to-digital Converter (TDC)

- Quantized phase detector with resolution of about 20 ps
- DCO clock passes through the inverter chain
- Delayed outputs are sampled by FREF

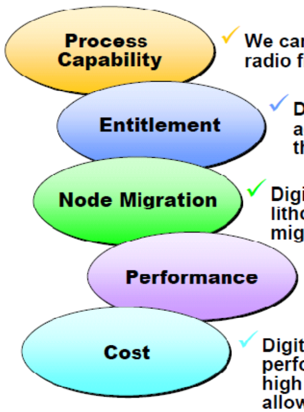


Production Testing Simplification

- Extensive use of built-in-testing capabilities to reduce test costs.
- Tester is simple (low cost) and test time is minimal.



The DRP Technology - Summary



- ✓ We can now clock digital logic at radio frequencies
- ✓ Digital technology takes advantage of advanced logic capability (and leverages the wafer process technology investment)
- ✓ Digital systems scale with lithography and are easy to migrate
- ✓ Performance improves with new technology, the job keeps getting easier
- ✓ Digital radios offer excellent performance, low power consumption, high manufacturing yield, and low cost; allow built-in self test and calibration