# Physics and Engineering of CMOS Devices

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**Review of the Last Lecture (1)** 



Two pn junctions are connected in series. One is reversely biased and the other is forward biased.



Positive gate bias generates surface inversion layer, which forms Ohmic contacts with source/drain diffusion layers.

### **Review of the Last Lecture (2)**

By introducing threshold voltage  $(V_{th})$ , Poisson's equation can be replaced by the following equation.

$$-qn_{l} = -WC_{g}\left(V_{g} - V_{th}\right)$$
Source
$$V(y)$$

$$V(y)$$

$$V_{th} \longrightarrow V_{th} + V\left(y\right)$$

$$I_{d} = WC_{g}\left(V_{g} - V(y) - V_{th}\right)\mu_{e}\frac{dV\left(y\right)}{dy}$$

$$I_{d}dy = WC_{g}\left(V_{g} - V(y) - V_{th}\right)\mu_{e}dV\left(y\right)$$
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$$Review of the Last Lecture (3)$$

$$\int_{0}^{L} I_{d}dy = \int_{0}^{V_{d}}WC_{g}\left(V_{g} - V(y) - V_{th}\right)\mu_{e}dV\left(y\right)$$

$$I_{d} = \mu_{e}C_{g}\frac{W}{L}\left[\left(V_{g} - V(y) - V_{th}\right)V_{d} - \frac{1}{2}V_{d}^{2}\right] \qquad (1)$$
Eq (1) is not valid when  $V_{d}$  is greater than  $V_{g}$ - $V_{th}$ .

q (1) is not valid when  $V_d$  is greater than  $V_g V_{th}$ .  $I_d = WC_g (V_g - V(y) - V_{th}) \mu_e \frac{dV(y)}{dy}$ When  $V_d > V_g - V_{th} (V_g - V_d - V_{th} < 0)$ 

Because in the depletion condition the equation above suggests hole accumulation! This is not true.

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# **Review of the Last Lecture (4)**



Carriers reaching at the pinchoff point are immediately transferred to the drain. Therefore, the current is obtained by integrating the formula from source to the pinch-off point.

 $I_{d} = \mu_{e}C_{g}\frac{W}{L}\left[\left(V_{g} - V_{th}\right)V_{d} - \frac{1}{2}V_{d}^{2}\right] \qquad \left(V_{d} \leq V_{g} - V_{th}\right)$ (1)  $I_{d} = \frac{1}{2}\mu_{e}C_{g}\frac{W}{L - \Delta L}\left(V_{g} - V_{th}\right)^{2} \qquad \left(V_{d} > V_{g} - V_{th}\right)$ (2)

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**Review of the Last Lecture (5)** 



Implicit assumptions are

- Constant mobility
- Linea relationship between velocity versus field

Insufficient treatments are as follows.

• Extremely simple formula,  $Q = C_g(V_g - V_{th})$  is used to derive potentialcharge relationship; the effect of impurity ions on electric field as well as potential has not been taken into account (no-depletion condition).

Accurate relationship between Q and V should be obtained. Physics and Engineering of CMOS Devices, Ken Uchida, Tokyo Tech, April 15, 2009

### **Depletion Approximation**

Effect of substrate impurity

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## Brief Review of Semiconductor Physics Bulk Bandstructure



# **Brief Review of Semiconductor Physics**

### **MOS Structure**

#### Flat-band condition

Vacuum Level





$$q\phi_m = q\chi + \frac{E_g}{2} + q\phi_F$$

 $E_{c}$  $q\phi_m < q\chi + \frac{E_g}{2} + q\phi_F$  $V_{FB} = \phi_m - \chi - \frac{E_g}{2q} - \phi_F$ 

Flat band voltage, V<sub>FB</sub> is the gate-tosubstrate voltage necessary to realize flatband condition. 9

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# **MOS Capacitor: Operation**



Nagative Gate Voltage

# MOS Capacitor: $\phi_s$ versus $Q_{depl}$



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# MOS Capacitor: $\phi_s$ versus $Q_{depl}$



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# MOS Capacitor: $\phi_s$ versus $Q_{depl}$ –cont'd

#### Electric Field at the surface, $F_s$ .





Depletion region has the capacitance.



As  $N_A$  increases, depletion capacitance,  $C_d$ , increases. This is due to the reduction of depletion layer width.

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# **Solving Poisson's Equation**

### Accumulation and Inversion Conditions

### **Brief Review of Semiconductor Physics**

### **Bulk Bandstructure**



Suppose that substrate is p-type with acceptor concentration of  $N_A$ .

$n_{p0} p_{p0} = n_i^2$ $n_{p0} N_A \approx n_i^2$	$N_A \approx p_{p0} = n_i \exp\left(\frac{q\phi_F}{k_B T}\right)$	(6)
$n_{p0} \approx \frac{n_i^2}{N_A}$	$\frac{n_i^2}{N_A} \approx n_{p0} = n_i \exp\left(-\frac{q\phi_F}{k_B T}\right)$	(7) <u>1</u> 5

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## **Brief Review of Semiconductor Physics** Bandstructure at Semiconductor Surface



 $n_{\rm s}$ : electron concentration at the surface  $p_s$ : hole concentration at the surface  $N_A$ : acceptor concentration

$$n_{s} = n_{i} \exp\left(\frac{q\left(\phi_{s} - \phi_{F}\right)}{k_{B}T}\right)$$
$$= n_{i} \exp\left(-\frac{q\phi_{F}}{k_{B}T}\right) \exp\left(\frac{q\phi_{s}}{k_{B}T}\right)$$
$$n_{s} = \frac{n_{i}^{2}}{N_{A}} \exp\left(\frac{q\phi_{s}}{k_{B}T}\right) \qquad (8)$$
$$p_{s} = n_{i} \exp\left(\frac{q\left(\phi_{F} - \phi_{s}\right)}{k_{B}T}\right)$$
$$p_{s} = N_{A} \exp\left(-\frac{q\phi_{s}}{k_{B}T}\right) \qquad (9)$$

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# MOS Capacitor: $\phi_s$ versus $Q_s$

We will solve Poisson's equation.

$$\frac{d^2\phi}{dx^2} = -\frac{q}{\kappa_s \varepsilon_0} \left( N_D - N_A + p_p - n_p \right)$$
$$= -\frac{q}{\kappa_s \varepsilon_0} \left[ -N_A - \frac{n_i^2}{N_A} \exp\left(\frac{q\phi}{k_B T}\right) \right] \qquad N_D \approx 0$$
$$p_p \approx 0$$

Multiplying both sides by  $(d\phi/dx)dx$ , we will obtain

$$\frac{1}{2}\left(\frac{d\phi}{dx}\right)^{2} = \frac{qN_{A}}{\kappa_{s}\varepsilon_{0}}\left[\phi + \frac{k_{B}T}{q}\left(\frac{n_{i}}{N_{A}}\right)^{2}\left[\exp\left(\frac{q\phi}{k_{B}T}\right) - 1\right]\right]$$

$$Q_{s} = -\kappa_{s}\varepsilon_{0}E_{s} = -\sqrt{2qN_{A}}\kappa_{s}\varepsilon_{0}\left[\phi + \frac{k_{B}T}{q}\left(\frac{n_{i}}{N_{A}}\right)^{2}\left[\exp\left(\frac{q\phi}{k_{B}T}\right) - 1\right]\right]^{1/2} (10)$$

$$electrons + substrate impurity$$
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# MOS Capacitor: $\phi_s$ versus $Q_s$ –cont'd

Of course, we can include  $p_p$ .

$$\frac{d^2\phi}{dx^2} = -\frac{q}{\kappa_s \varepsilon_0} \left[ -N_A + N_A \exp\left(-\frac{q\phi}{k_B T}\right) - \frac{n_i^2}{N_A} \exp\left(\frac{q\phi}{k_B T}\right) \right]$$

$$\frac{1}{2}\left(\frac{d\phi}{dx}\right)^2 = \frac{qN_A}{\kappa_s\varepsilon_0} \left[\phi - \frac{k_BT}{q} \left[\exp\left(-\frac{q\phi}{k_BT}\right) - 1\right] + \frac{k_BT}{q} \left(\frac{n_i}{N_A}\right)^2 \left[\exp\left(\frac{q\phi}{k_BT}\right) - 1\right]\right]$$

$$Q_{s} = \mp \sqrt{2qN_{A}\kappa_{s}\varepsilon_{0}} \left[ \phi - \frac{k_{B}T}{q} \left[ \exp\left(-\frac{q\phi}{k_{B}T}\right) - 1 \right] + \frac{k_{B}T}{q} \left(\frac{n_{i}}{N_{A}}\right)^{2} \left[ \exp\left(\frac{q\phi}{k_{B}T}\right) - 1 \right] \right]^{1/2}$$
  
electrons + holes + substrate impurity (11)

# MOS Capacitor: $\phi_s$ versus $Q_s$



When  $\phi_s = 2\phi_F$ , the minority carrier density at the surface is comparable to the depletion charge density. Therefore,  $\phi_s$  of  $2\phi_F$ is defined as the threshold. When  $\phi_s$  is in the range from  $\phi_F$  to  $2\phi_F$ , the condition is called the weak inversion. When  $\phi_s$  is greater than  $2\phi_F$ , the condition is called the strong inversion.

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# MOS Capacitor: $\phi_s$ versus $Q_s$

$$\phi_s = 2\phi_F$$

At  $\phi_s = 2\phi_F$ , the minority carrier density at the surface is equal to the majority carrier density in the substrate;  $n_s = N_A$ 

The threshold voltage, where the surface condition changes from the weak inversion to the strong inversion, is defined as,

$$V_{th} = V_{FB} + 2\phi_F + \frac{\sqrt{4qN_A\kappa_s\varepsilon_0\phi_F}}{C_{ox}}$$
(12)  
Voltage drop within Si substrate Voltage drop within gate oxide

# Non-equilibrium condition

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## Quasi-Fermi Level in non-equilibrium Semiconductor

In equilibrium semiconductors, Fermi energy level ( $E_F$ ) is defined either by the electron density and the hole density. In other words, both electron and hole densities can calculated using the Fermi energy level.

However, in non-equilibrium semiconductors, the single  $E_F$  is not enough to describe carrier numbers. For example, in light-illuminated semiconductors, many electrons and holes are populated. In those non-equilibrium semiconductors,  $E_F$  for electrons should be closer to the conduction band than to the valence band in order to generate appropriate number of electrons with  $n_i \exp(E_i - E_F / k_B T)$ , whereas  $E_F$  for holes should be closer to the valence band. Therefore, under non-equilibrium condition, Fermi energy level for electrons and that for holes should be defined separately, based on the number of electrons and holes respectively.

These Fermi energy levels are called qusi-Fermi energy levels. For electrons and holes, they are written as  $E_{Fn}$  and  $E_{Fn}$ , respectively.

# **PN Junction**



A biased PN junction is another example of the non-equilibrium semiconductor.

In the depletion layer, we have  $E_{Fn}$  for electrons and  $E_{Fp}$  for holes.

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## **Gated PN Junction**



In gated PN junctions, we have  $E_{Fn}$  for electrons and  $E_{Fp}$  for holes when the junction is biased.

The point is that in the depletion region  $E_{Fn}$  should be used to calculate the electron densities.

# Gated PN Junction –cont'd



$$V_{th} = V_{FB} + 2\phi_F + V_R + \frac{\sqrt{2qN_A\kappa_s\varepsilon_0\left(2\phi_F + V_R\right)}}{C_{ox}}$$
(13)

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# Summary

- Depletion approximation is introduced to derive  $\phi_s$  versus  $Q_{depl}$  characteristics.
- In the MOS structure, Poisson's equation is solved. The equations representing accumulation, depletion, weak-inversion, and strong-inversion are obtained.
- Quasi Fermi level is introduced to discuss carriers in non-equilibrium semiconductors.
- Carriers in the gated PN junction is discussed.

## Question

Consider MOS capacitor with gate oxide (SiO2) thickness of 10nm and substrate acceptor doping concentration of  $1x10^{16}$ cm<sup>-3</sup>. Suppose the substrate is grounded and the flat-band condition is realized when the gate voltage is 0V. Calculate the depletion layer width and the surface electric field when the gate voltage of 1V is applied to the MOS capacitor.

It should be assumed that the surface potential is fixed at  $2\phi_F$  if the gate voltage is greater than  $V_{th}$ . The inversion charges  $Q_{inv}$  can be obtained by  $C_g(V_g-V_{th})$ .

The following constants and equations may be used.

 $\kappa_{SiO2} = 3.9$   $\kappa_{Si} = 11.9$   $\varepsilon_0 = 8.85 \text{ x } 10^{-12} \text{ F/m}$   $q = 1.6 \text{ x } 10^{-19} \text{ C}$   $n_i = 1.45 \text{ x } 10^{10} \text{ cm}^{-3}$  $k_B = 1.38 \text{ x } 10^{-23} \text{ J/K}$ 

$$\phi_F = \frac{k_B T}{q} \ln\left(\frac{N_A}{n_i}\right)$$

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