Physics and Engineering of CMOS Devices

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Requirements

- Basics of Quantum Mechanics
  – Quantum Confinement Effects
  – Scattering of electrons with phonons etc.
- Electromagnetic
  – Gauss's Law
  – Poisson's Equation
- Fundamentals of Solid-State Physics
  – Band Structure of Semiconductors (Effective Mass, Density of States etc.)
  – Basics of Semiconductor Physics (pn junctions, semiconductor statistics)

Class Objective

This class provides the fundamentals of advanced nanoscale MOS transistors. Firstly, the operation of MOS transistors fabricated on bulk Si substrate will be explained. The impact of shrinking device dimensions on device performance will be discussed. Then, the concept of equivalent scaling, which is important in modern MOS transistors, will be introduced. As an example of the equivalent scaling, mobility booster technologies and high-k&metal gate stack will be discussed. By taking this class, it is expected that students get familiar with physics and engineering of modern, advanced CMOS devices.

Class Schedule (Tentative)

- Fundamentals of MOSFETs (4 Classes)
- SOI MOSFETs (2 Classes)
- Strained MOSFETs (2 Classes)
- MOSFETs with High-κ Gate Dielectrics (1 Class)
- High-Mobility Channel MOSFETs (1Class)
- Fabrication Process (1 Class)
- Reliability and Variability (1 Class)
- Other Advanced Topics (1 Class)

Class Schedule –cont'd

- Fundamentals of MOSFETs (4 Classes)
  - Simple Analytical MOSFET Model
  - MOS Capacitor
  - MOSFET Models (Charge Sheet Model)
  - Scaling Strategy of MOSFETs
  - Mobility and Velocity of Charged Carriers
  - Quantum Mechanical Effects
  - Ballistic FETs
  - Basics of Semiconductor Physics

Grading

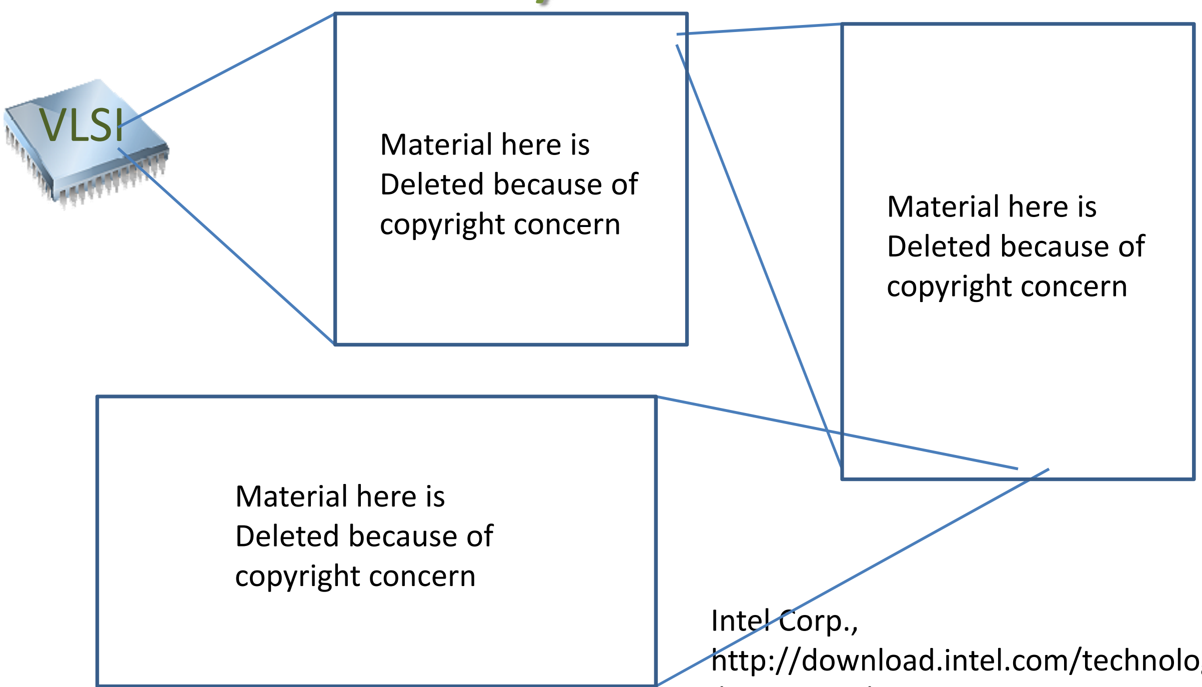
- Exercises during the class (40%)
- Term-end Examination (60%)

Application of VLSIs

VLSIs are applied to wide area of application domains!

VLSI: Very Large Scale Integrated Circuits

MOSFETs as Key Elements in VLSIs



Intel Corp., http://download.intel.com/technology/iedm2007/HiKMG_pres.pdf

MOSFETs are key components of VLSI, where they are working as switches to perform logic operations.

Moore's Law

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Source: Intel (http://www.intel.com), from presentation at ISSCC 2003

Moore's Law –cont'd

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Moore's Law –cont'd

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Evolution of Processors

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36-Year Evolution

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1971
Intel 4004 Processor
108kHz Clock
10um Technology

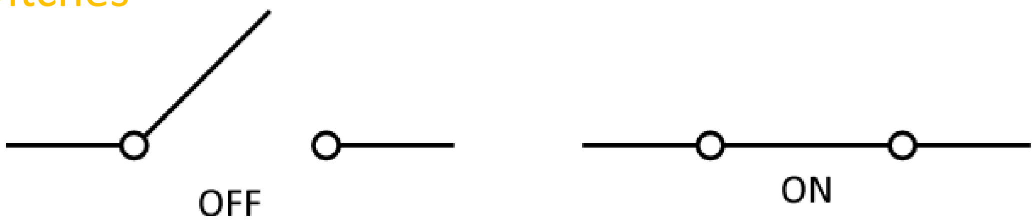
2007
Intel Quad-Core Xeon Processor
>3GHz Clock
0.045um Technology

Source: Intel Corp.(http://www.intel.com)

MOSFETs as Switches in VLSIs

Ideal switch has infinite resistance in the off state, whereas zero resistance in the on state.

Ideal Switches

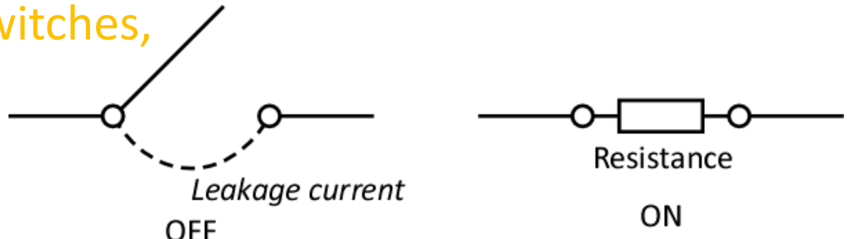


Infinite Resistance

Zero Resistance

In reality, switches have leakage current in the off state and finite resistance is observed in the on state.

Realistic Switches,



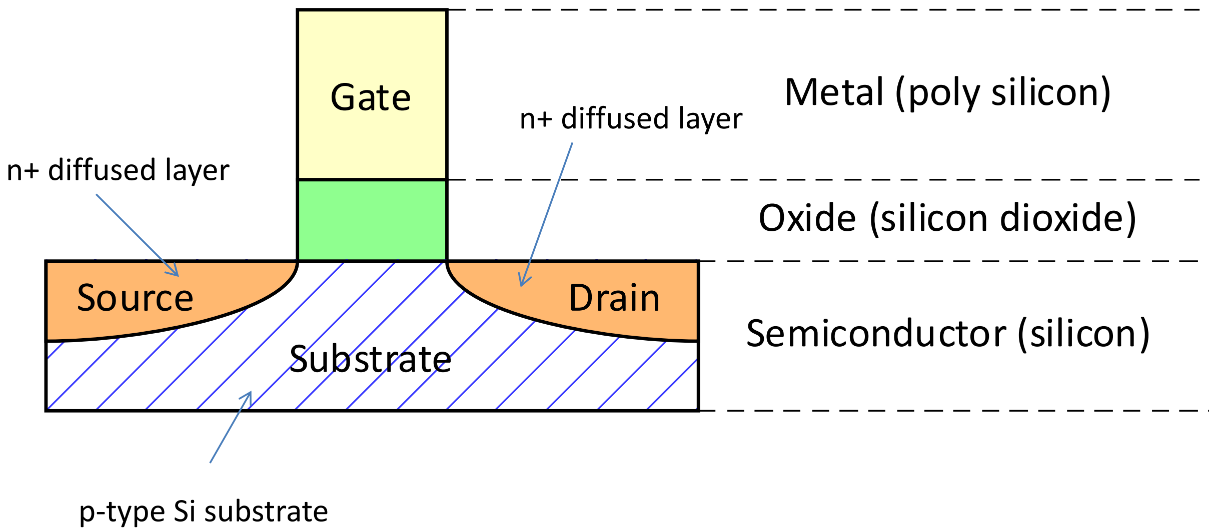
Strategy to Enhance VLSI Performance

Requirements against Switches

- Reduction in ON resistance.
- Reduction in dimensions.
- Reduction in leakage current.

The performance of MOSFETs are improved by reducing transistor dimensions (sizes), while keeping leakage current as small as possible.

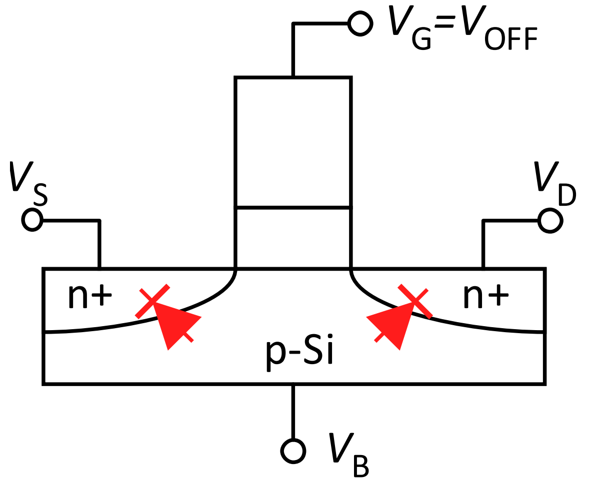
Structure of MOSFETs



- Metal-Oxide-Semiconductor Structure
- Field-Effect Transistor

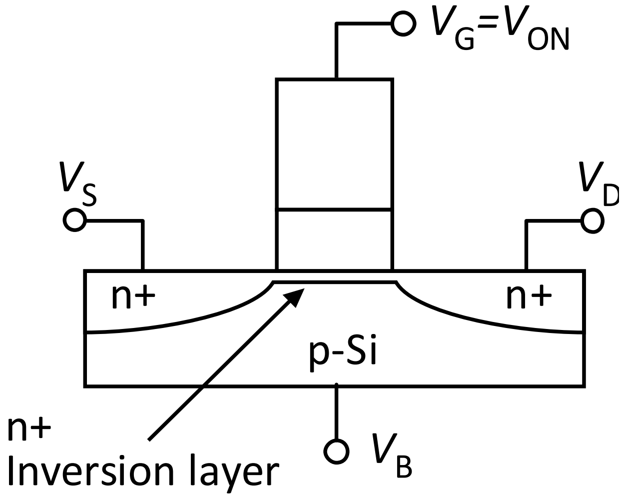
Schematics of MOSFET Operation

OFF State



Two pn junctions are connected in series. One is reversely biased and the other is forward biased.

ON State



Positive gate bias generates surface inversion layer, which forms Ohmic contacts with source/drain diffusion layers.

Basic Equations for Describing MOSFET Characteristics

- Poisson's Equation

$$\nabla^2 \phi = -\frac{\rho}{\kappa_s \varepsilon_0}$$

- Carrier Transport Equation

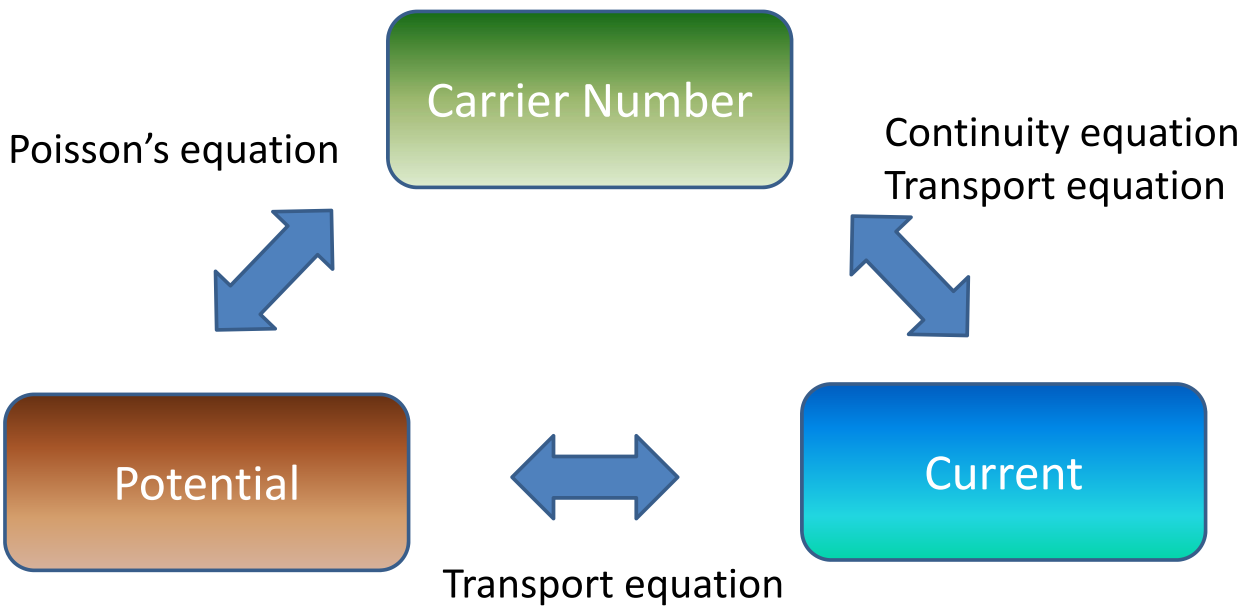
$$\mathbf{J}_n = q\mu_n n\mathbf{E} + qD_n \nabla n$$

- Current Continuity Equation

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla \mathbf{J}_n - R_n + G_n$$

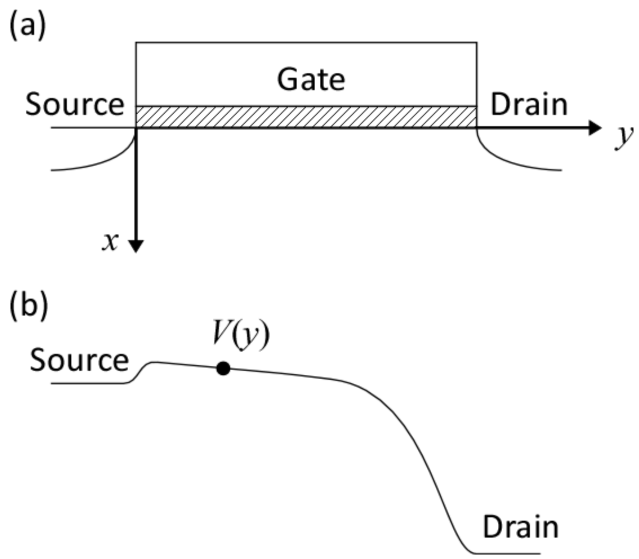
ϕ: potential
ρ : charge density
κ_s : dielectric constant
ε_0 : permittivity in vacuum
μ_n : mobility
q : elemental charge
D_n : diffusion constant
G_n : generation rate
R_n : recombination rate

Basic Equations



These equations should be solved self-consistently; they are solved numerically.

Coordinate in MOSFETs



The origin is located at the source edge of the MOS interface.
The Y axis is located at the MOS interface and is along the channel direction.
The X axis is normal to the MOS interface.
The Z axis is at the MOS interface and is along the width direction.

Assumptions for deriving MOSFET Model

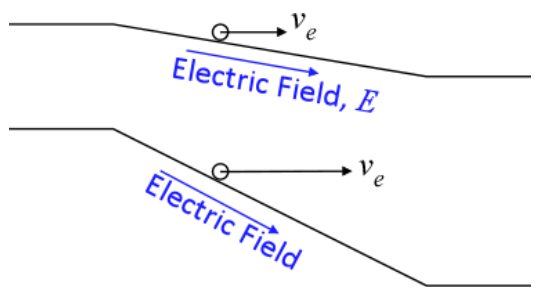
- Recombination and generation of carriers are negligible; current continuity equation is not taken into account.
- Diffusion current is much less than drift current.
- Normal Electric field is much greater than lateral electric field. (Gradual Channel Approximation: GCA)

$$\frac{\partial^2 \phi}{\partial x^2} \gg \frac{\partial^2 \phi}{\partial y^2}$$

Poisson's equation is reduced to

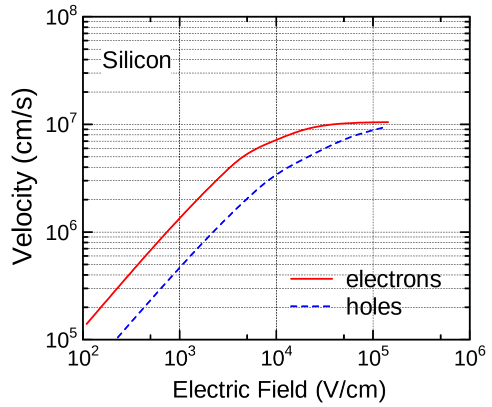
$$\frac{\partial^2 \phi}{\partial x^2} = -\frac{\rho}{\kappa_s \varepsilon_0}$$

Velocity and Mobility



The velocity of charged carriers (electrons, holes) is proportional to electric field.

$$v_e = \mu E$$



However, at electric field greater than 3×10^3 V/cm, the none-linearity is observed. This effect will be taken into account in later lectures.

Simple Analytical MOSFET Model (I)

$V_d \approx 0$

By introducing threshold voltage (V_{th}), Poisson's equation can be replaced by the following equation.

$$-qn_l = -WC_g\left(V_g - V_{th}\right)$$

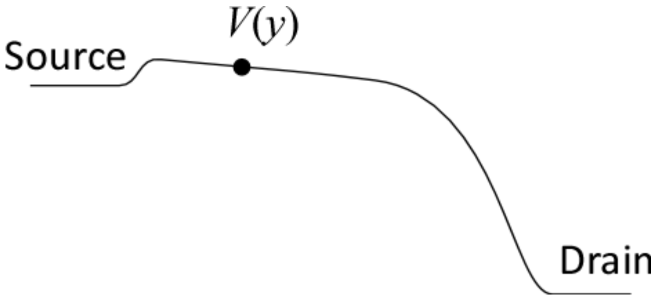
n_l: number of charges per unit length

$$\begin{aligned} I_d &= -qn_l\mu_e E \\ &= WC_g\left(V_g - V_{th}\right)\mu_e E \\ &= \mu_e C_g W\left(V_g - V_{th}\right)\frac{V_d}{L} \\ &= \mu_e C_g \frac{W}{L}\left(V_g - V_{th}\right)V_d \qquad \left(V_d \approx 0\right) \end{aligned}$$

This is valid when V_d is very small.

Simple Analytical MOSFET Model (II)

$V_d \neq 0$



$$V_{th} \longrightarrow V_{th} + V(y)$$

$$I_d = WC_g\left(V_g - V(y) - V_{th}\right)\mu_e \frac{dV(y)}{dy}$$

$$I_d dy = WC_g\left(V_g - V(y) - V_{th}\right)\mu_e dV(y)$$

Simple Analytical MOSFET Model (II) –cont'd

$$\int_0^L I_d dy = \int_0^{V_d} WC_g\left(V_g - V(y) - V_{th}\right)\mu_e dV(y)$$

$$\boxed{I_d = \mu_e C_g \frac{W}{L}\left[\left(V_g - V_{th}\right)V_d - \frac{1}{2}V_d^{\,2}\right] \qquad (1)}$$

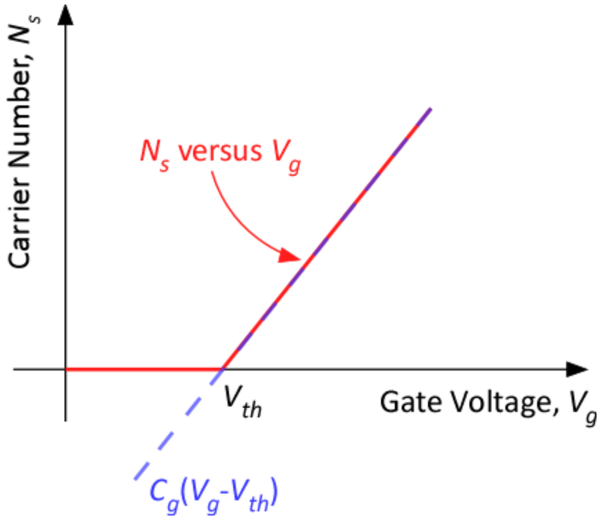
$$I_d = WC_g\left(V_g - V(y) - V_{th}\right)\mu_e \frac{dV(y)}{dy}$$

When

$V_d > V_g - V_{th}$ $\left(V_g - V_d - V_{th} < 0\right)$

Hole accumulation is suggested! This is not true.

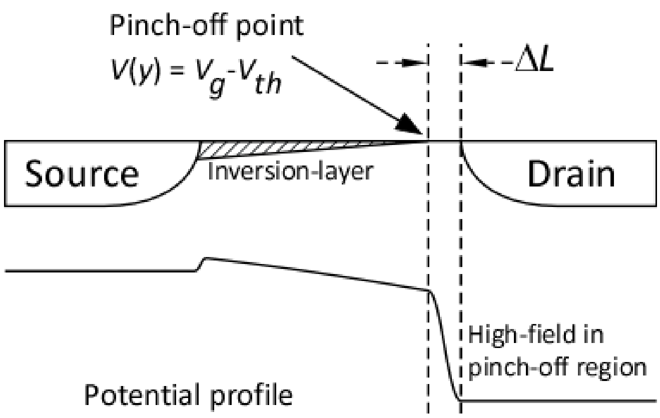
Simple Analytical MOSFET Model (II) –cont'd



In semiconductor, inversion-layer is formed when V_g is greater than V_{th}. If V_g is between V_{FB} and V_{th}, not hole accumulation layer but depletion layer is formed. Our simple equation, $C_g(V_g-V_{th})$, does not represent the depletion condition.

Eq. (1) is valid, when $V_d > V_g - V_{th}$

Simple Analytical MOSFET Model (II) –cont'd

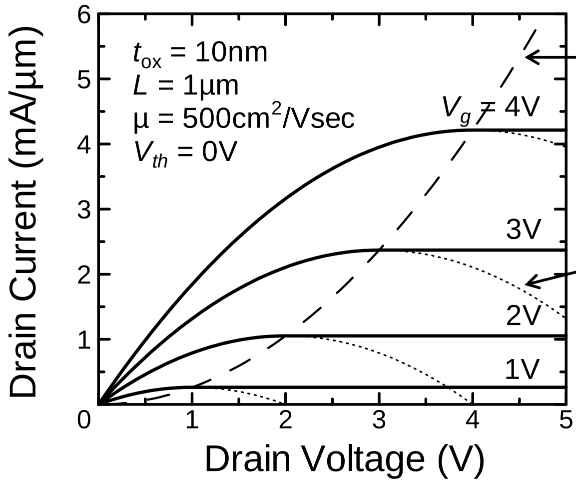


Carriers reaching at the pinch-off point are immediately transferred to the drain. Therefore, the current is obtained by integrating the formula from source to the pinch-off point.

$$I_d = \mu_e C_g \frac{W}{L}\left[\left(V_g - V_{th}\right)V_d - \frac{1}{2}V_d^{\ 2}\right] \qquad \left(V_d \le V_g - V_{th}\right) \quad (1)$$

$$I_d = \frac{1}{2}\mu_e C_g \frac{W}{L-\Delta L}\left(V_g - V_{th}\right)^2 \qquad \left(V_d > V_g - V_{th}\right) \quad (2)$$

Simple Analytical MOSFET Model –cont'd



$$I_d = \frac{1}{2}\mu_e C_g \frac{W}{L}\left(V_g - V_{th}\right)^2$$

$$I_d = \mu_e C_g \frac{W}{L}\left[\left(V_g - V_{th}\right)V_d - \frac{1}{2}V_d^{\,2}\right]$$

Implicit assumptions are

- Constant mobility
- Linea relationship between velocity versus field

Insufficient treatments are as follows.

- Distribution functions are not used to calculate carrier numbers.
- Effect of substrate impurity is not considered.
- One-dimensional electrostatics is used to calculate potential distribution.

Summary

- Equations to derive MOSFET characteristics are introduced.
  – Poisson's Equation
  – Carrier Transport Equation
  – Current Continuity Equation
- Simple MOSFET Model is derived.
  – GCA: Gradual Channel Approximation
  – No Diffusion Current
  – Q=C(V_g-V_{th}) is utilized.