Layout of CMOS VLSI Circuits

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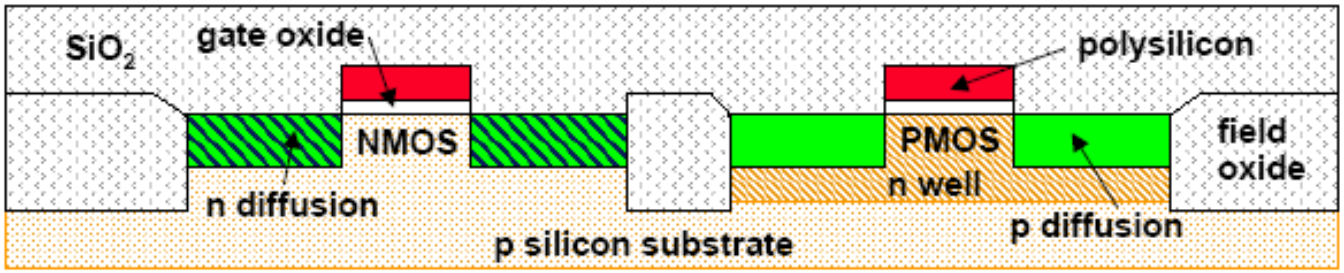
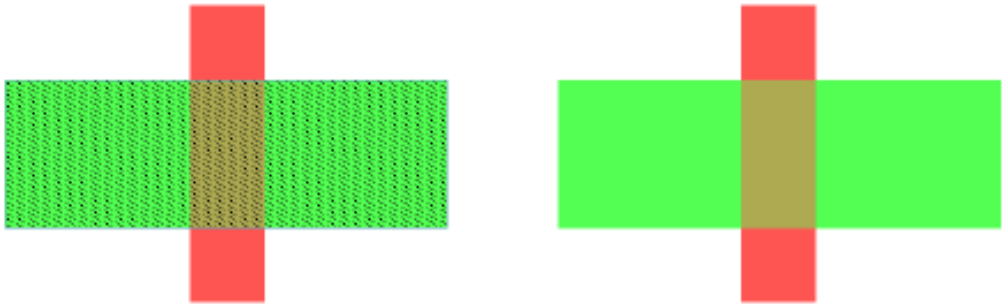
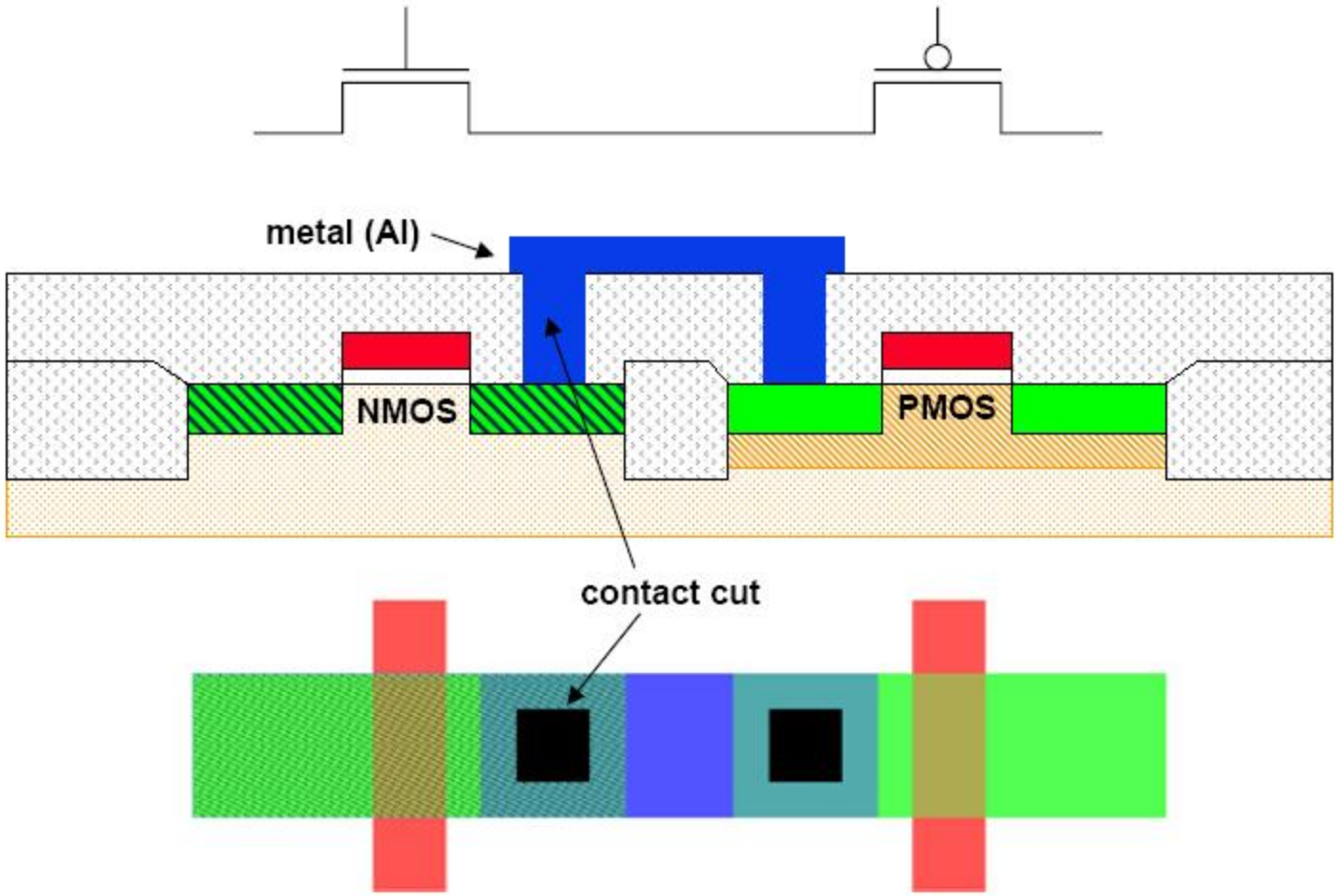
Simplified CMOS Process - Transistors

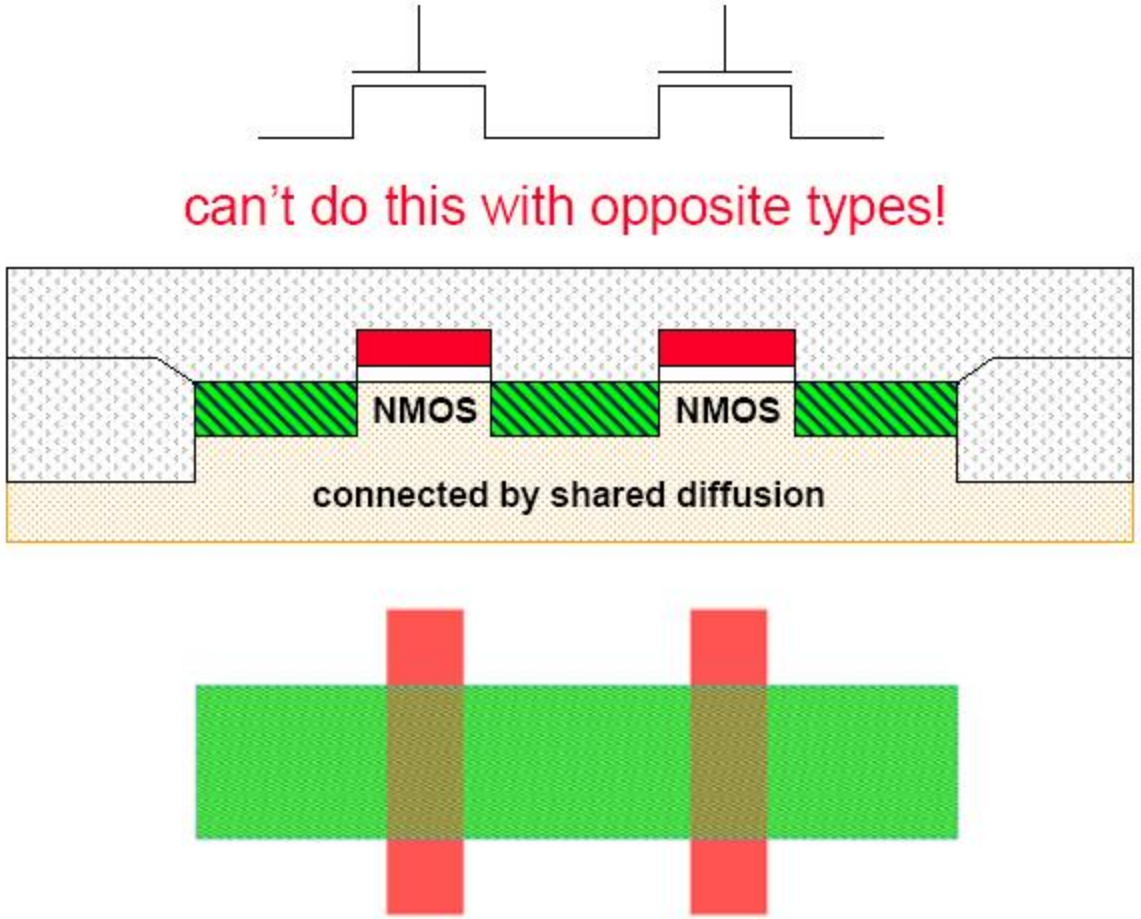




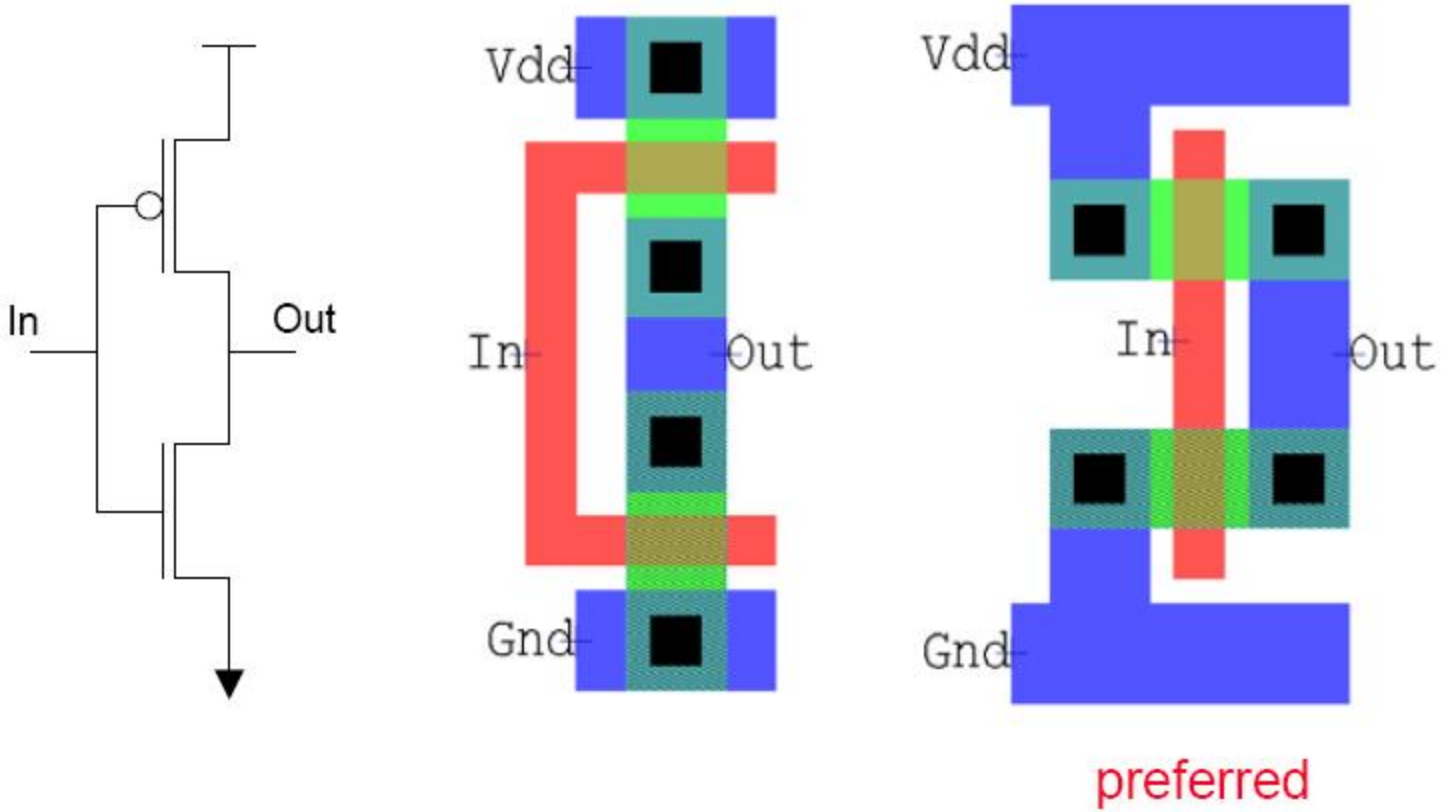
Metal P to N Connection



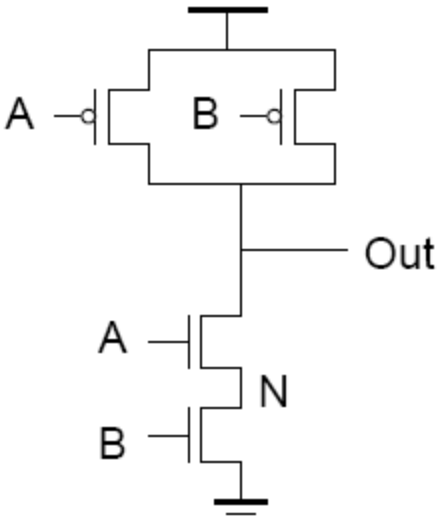
Serial Transistor Connection by Diffusion

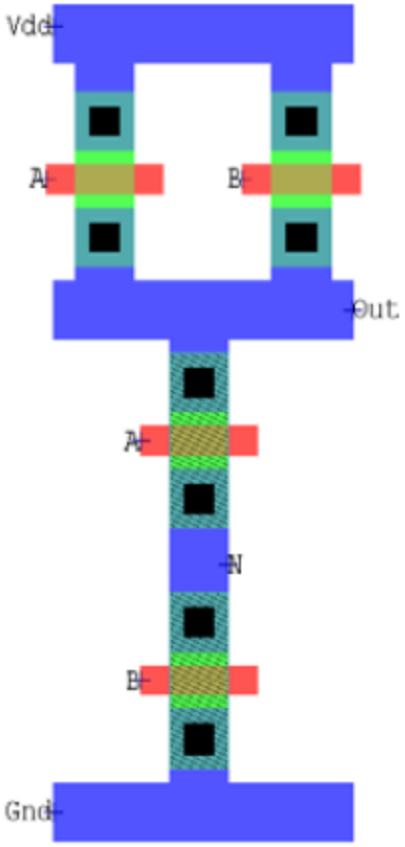


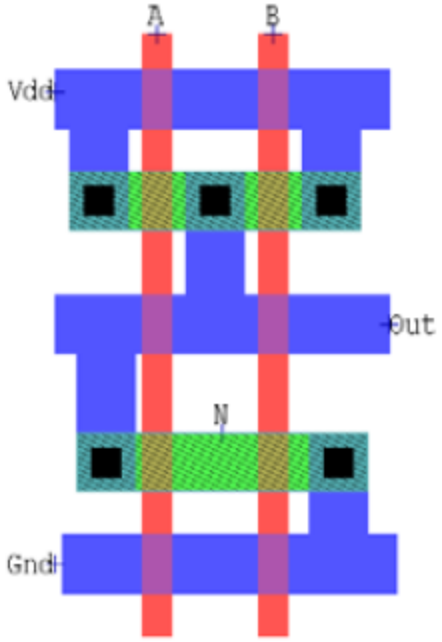
Layout of Inverter



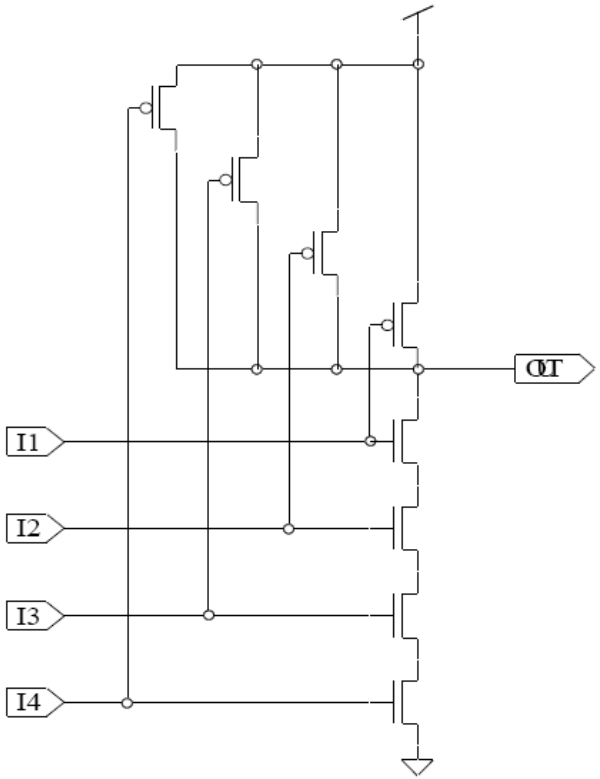
Layout of 2-Way NAND

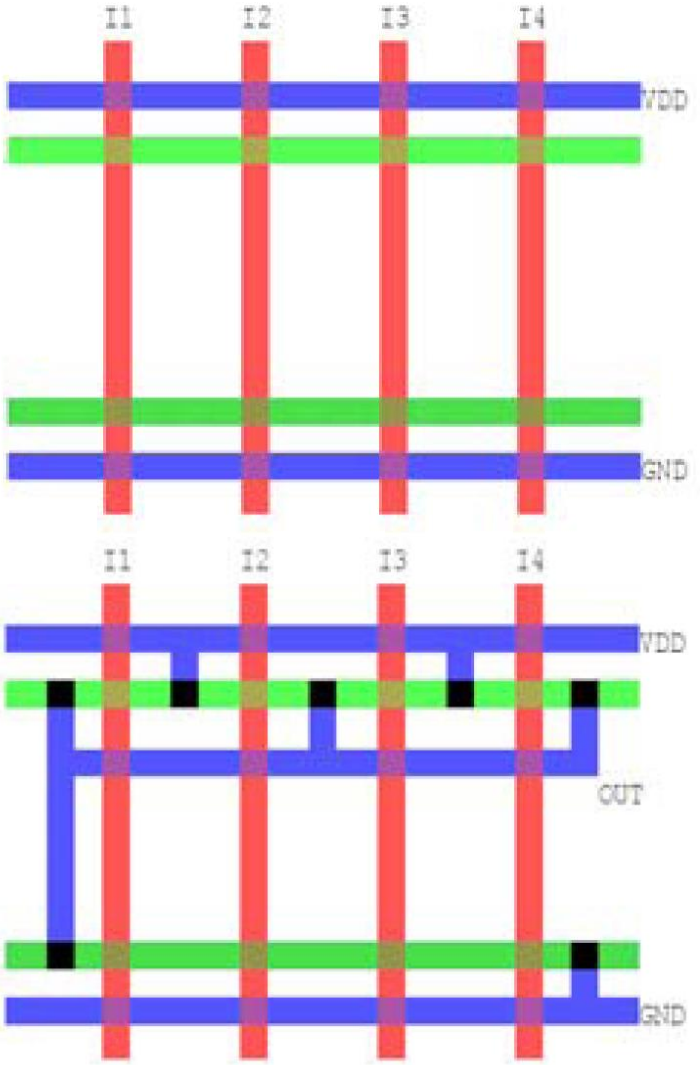




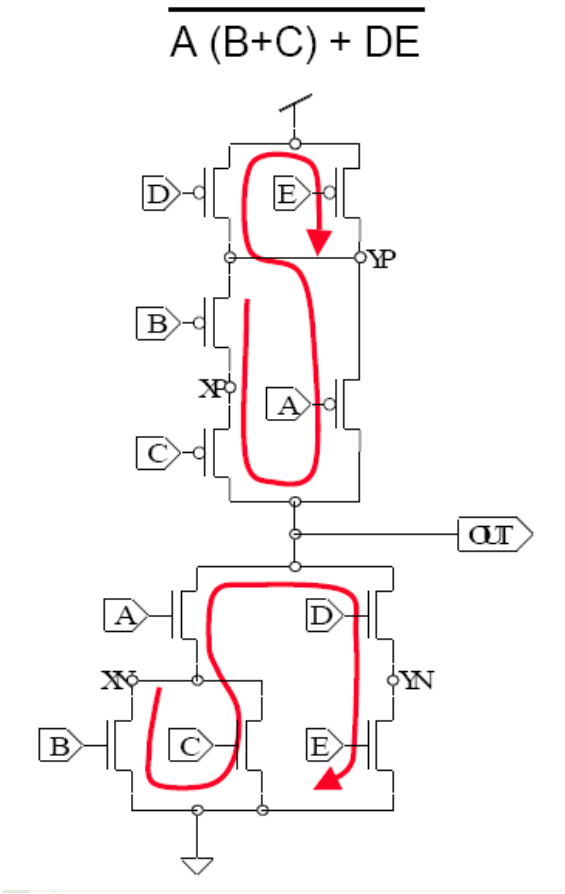


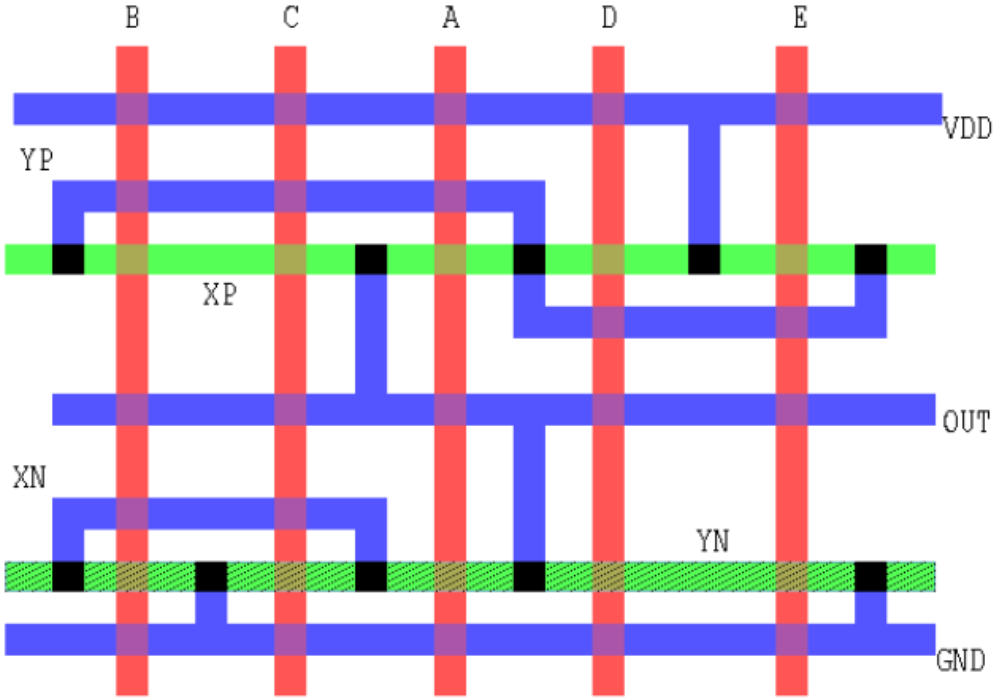
4-Way NAND Stick Layout



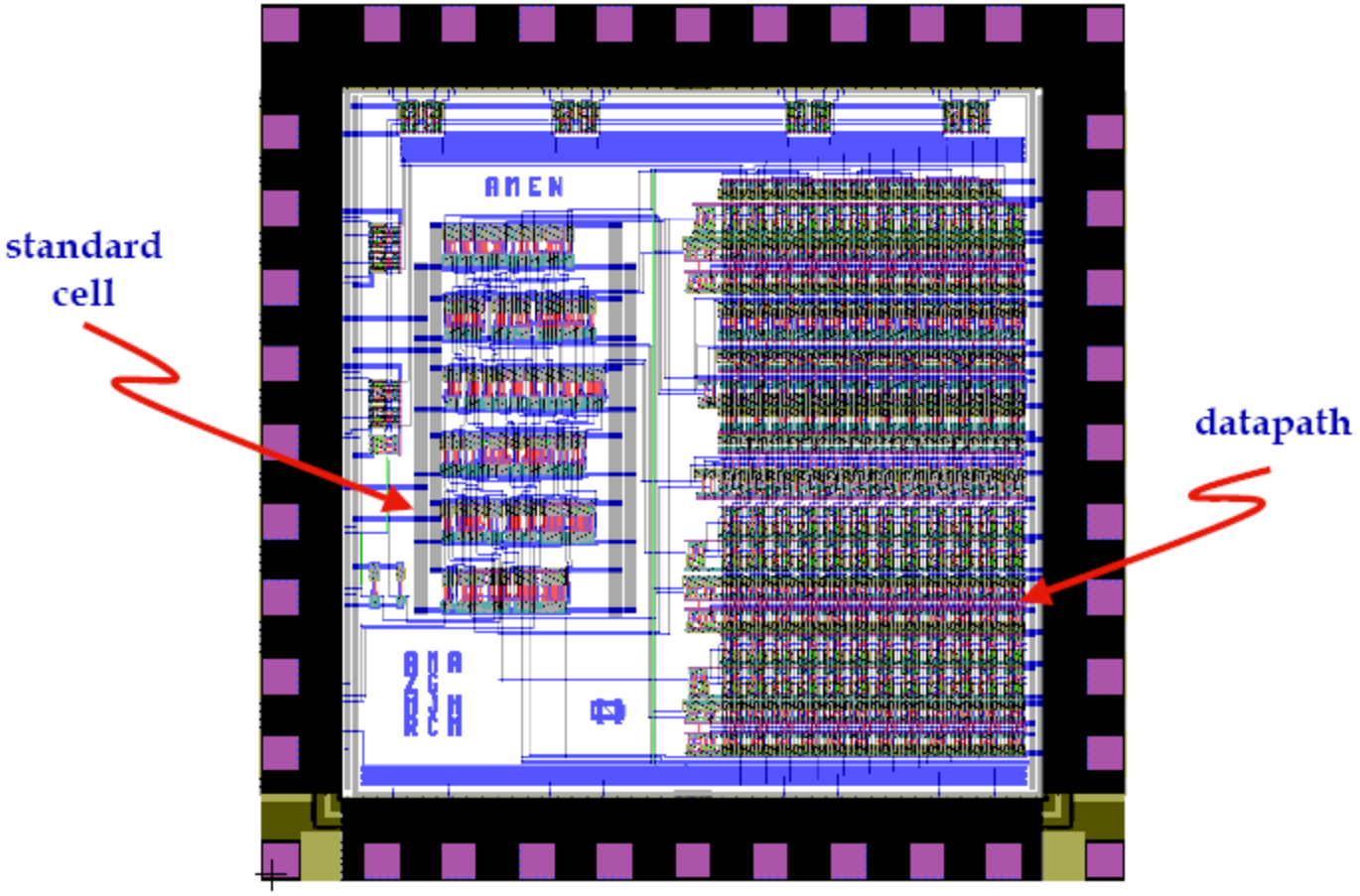


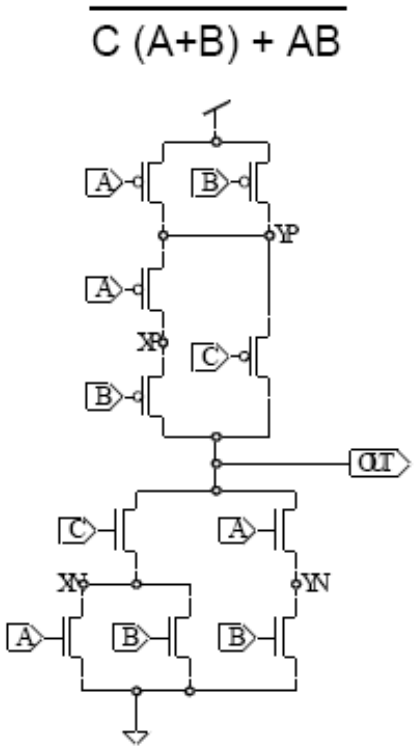
Layout of Compound Gates – Euler Path

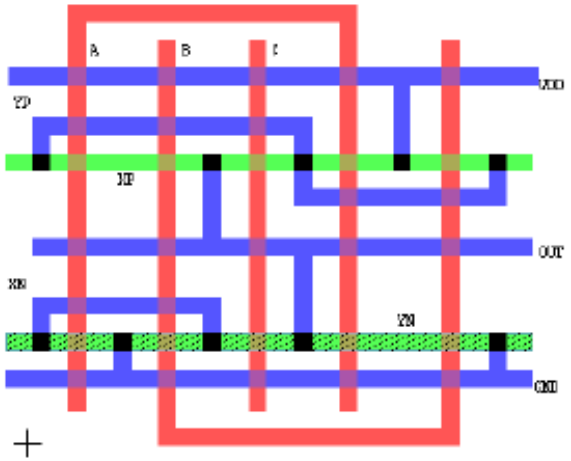




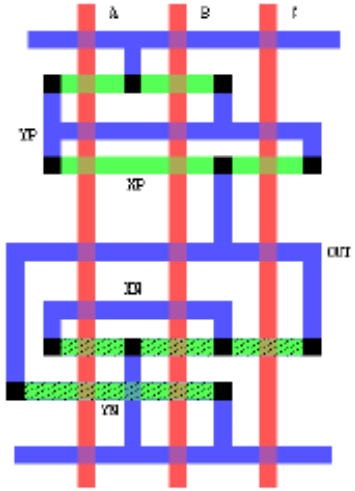
Layout Styles





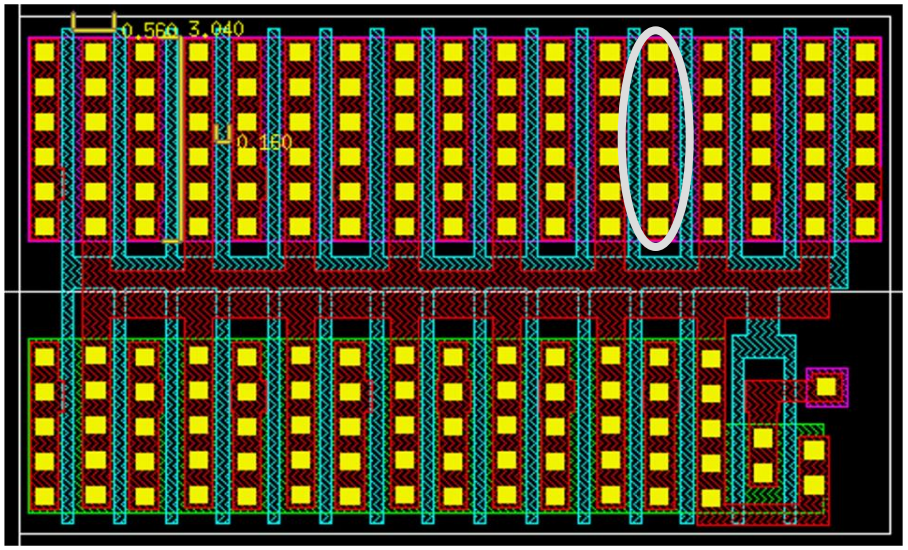


standard cell

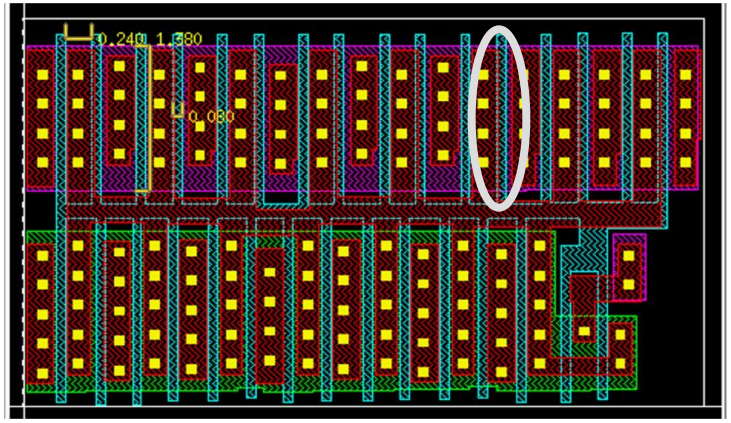


datapath

Layout in 130 and 90 Nanometers

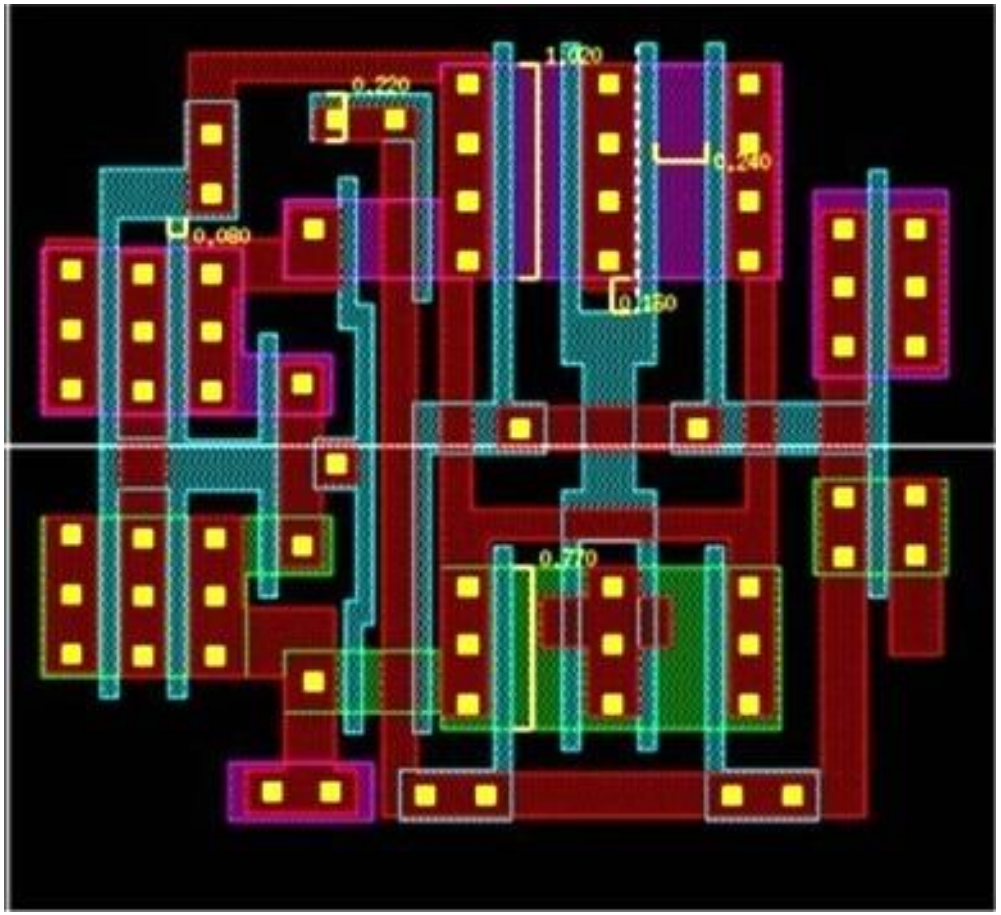


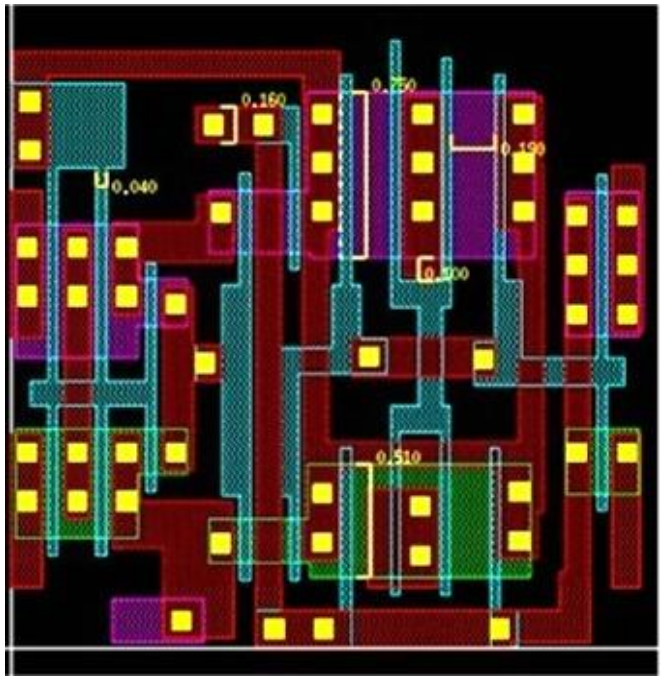
130nm



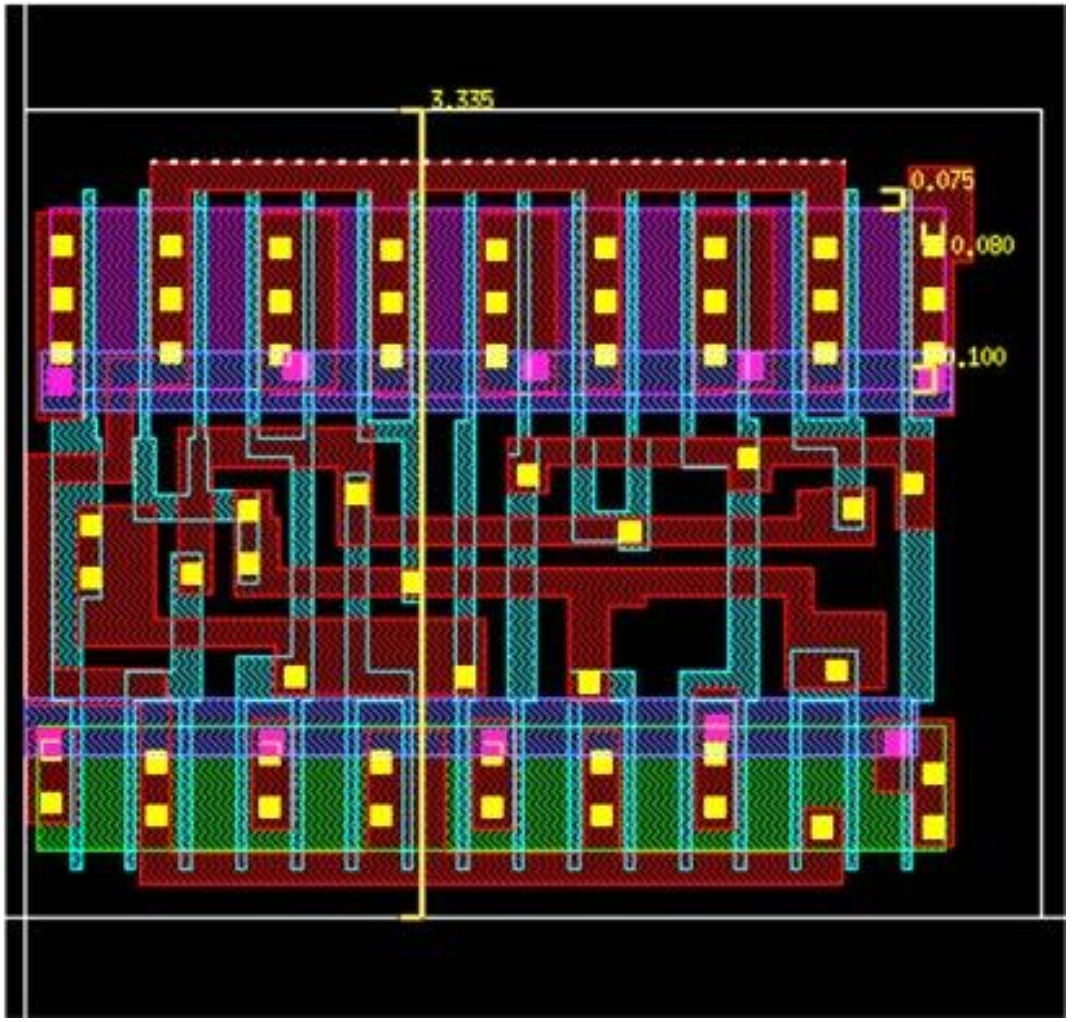
90nm

Layout in 90 and 65 Nanometers

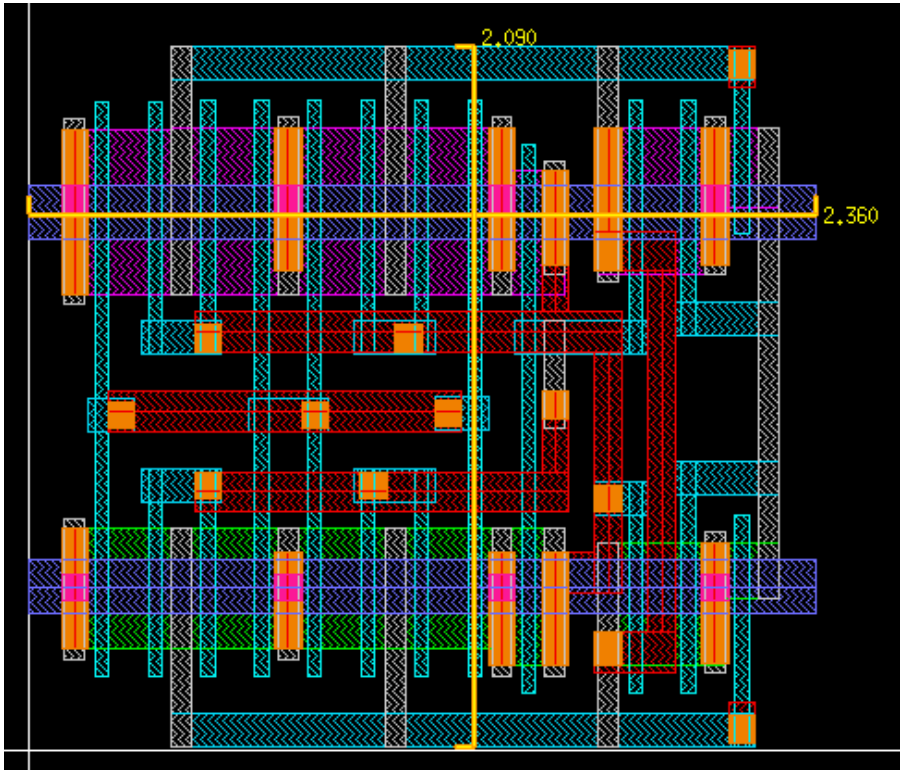


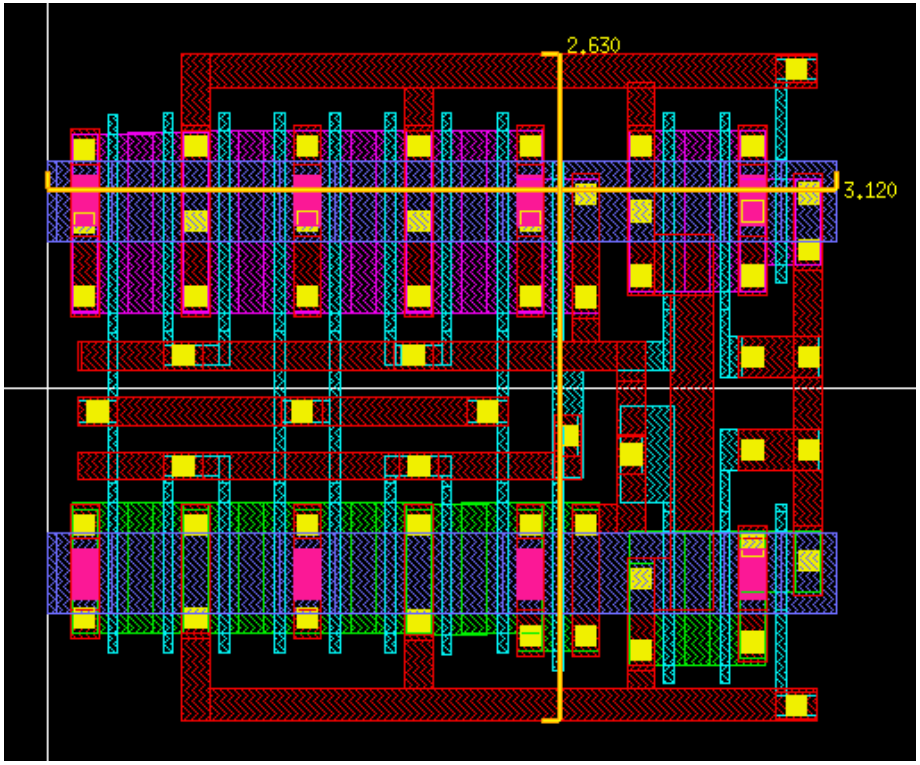


Layout in 65 Nanometers



Layout in 65 and 45 Nanometers





Possible Layout in 32 Nanometers