VLSI Floorplanning and Planar Graphs
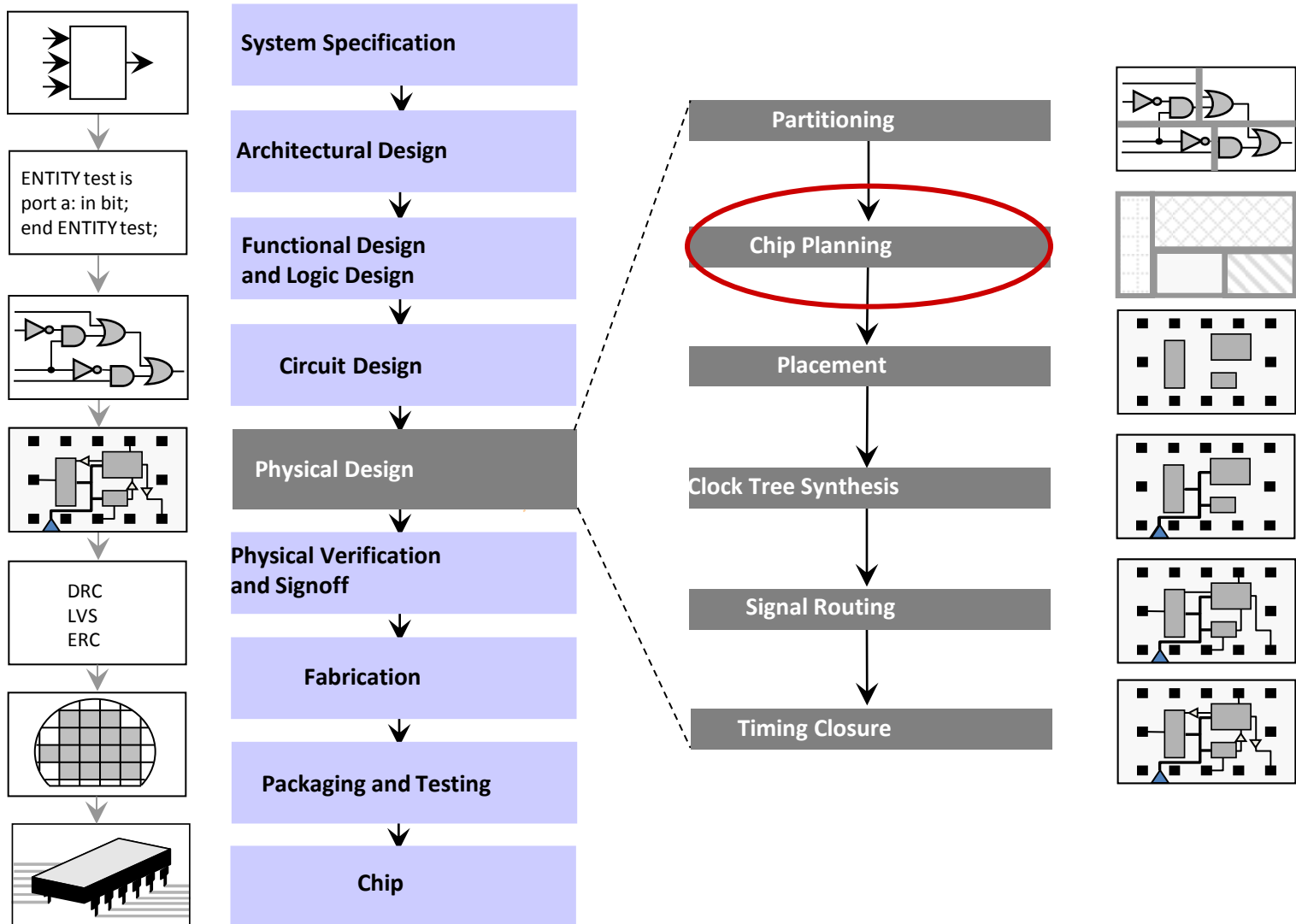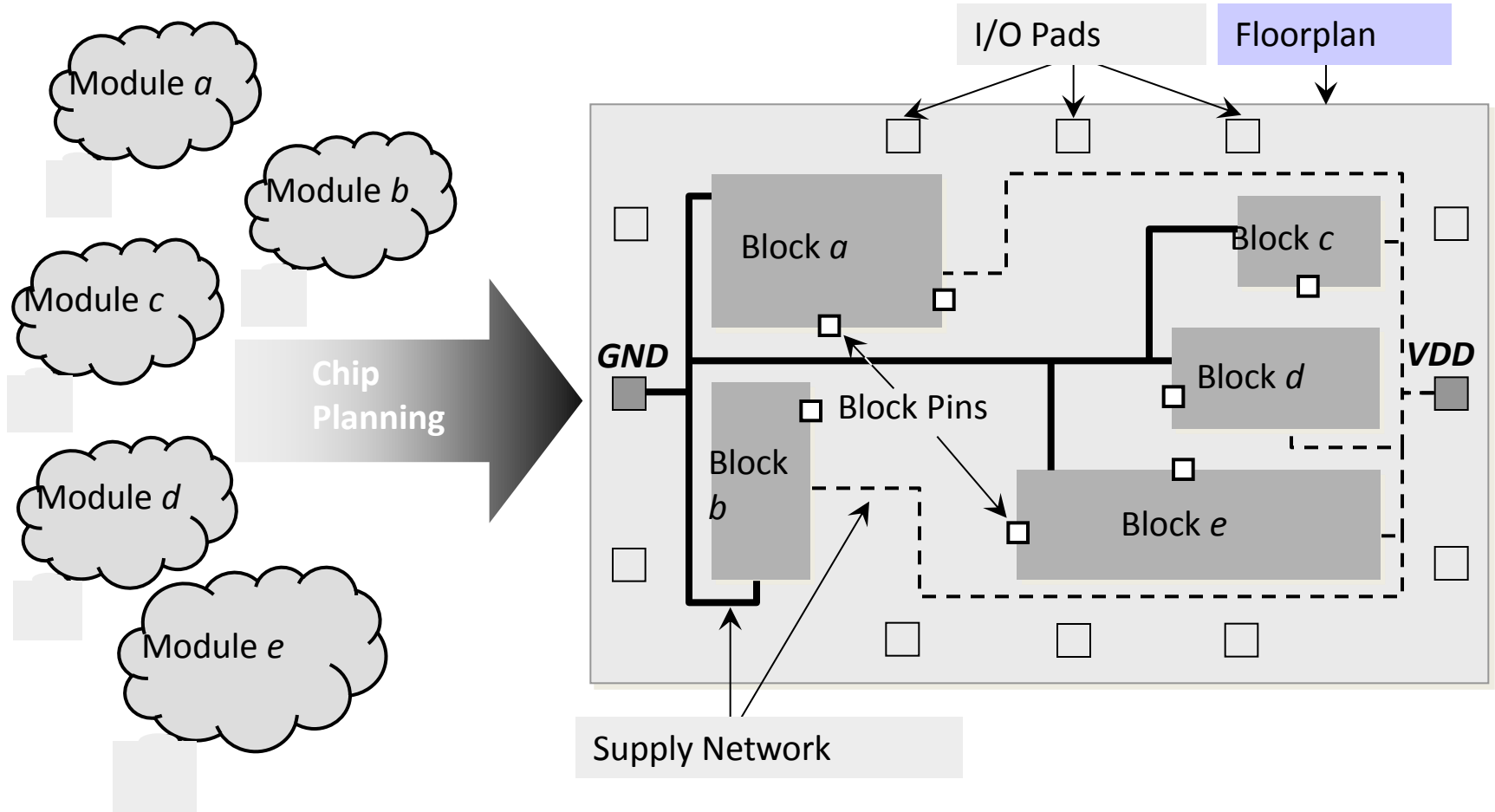
prepared and Instructed by
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System Specification

Architectural Design

Functional Design and Logic Design

Circuit Design

Physical Design

Physical Verification and Signoff

Fabrication

Packaging and Testing

Chip

ENTITY test is
port a: in bit;
end ENTITY test;

DRC
LVS
ERC

Partitioning

Chip Planning

Placement

Clock Tree Synthesis

Signal Routing

Timing Closure

VLSI Floor Planning and Planar Graphs

Module *a*

Module *b*

Module *c*

Module *d*

Module *e*

Chip
Planning

I/O Pads

Floorplan

Block *a*

Block *c*

GND

Block Pins

Block *d*

VDD

Block
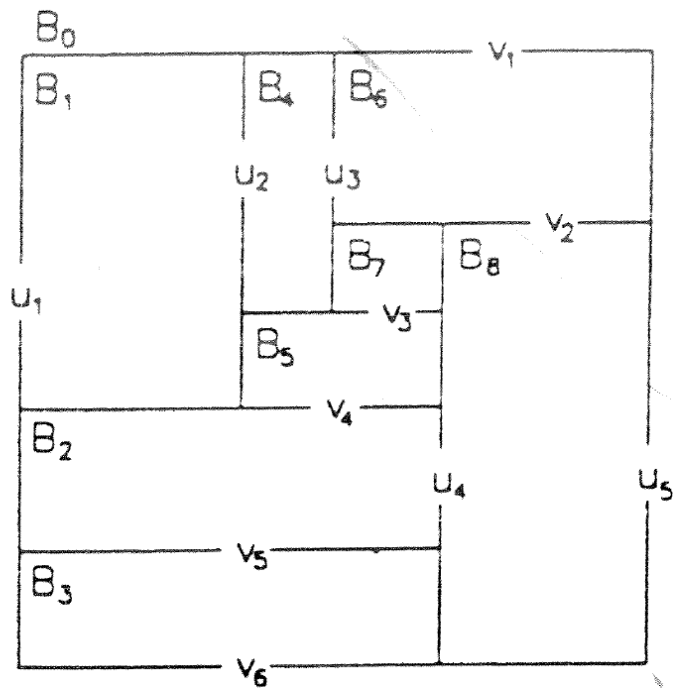*b*

Block *e*

Supply Network
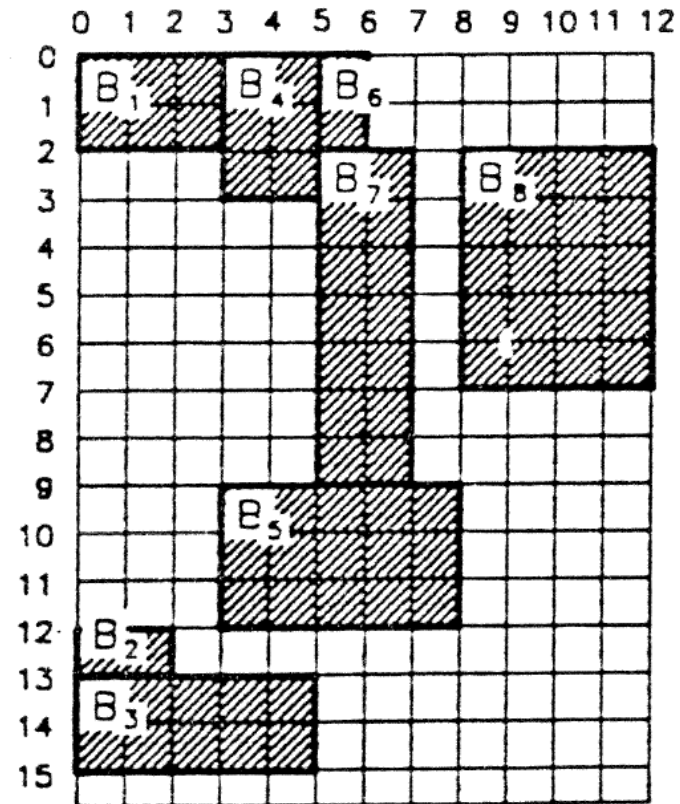
Fig. 1. Eight sub-rectangle floorplan.

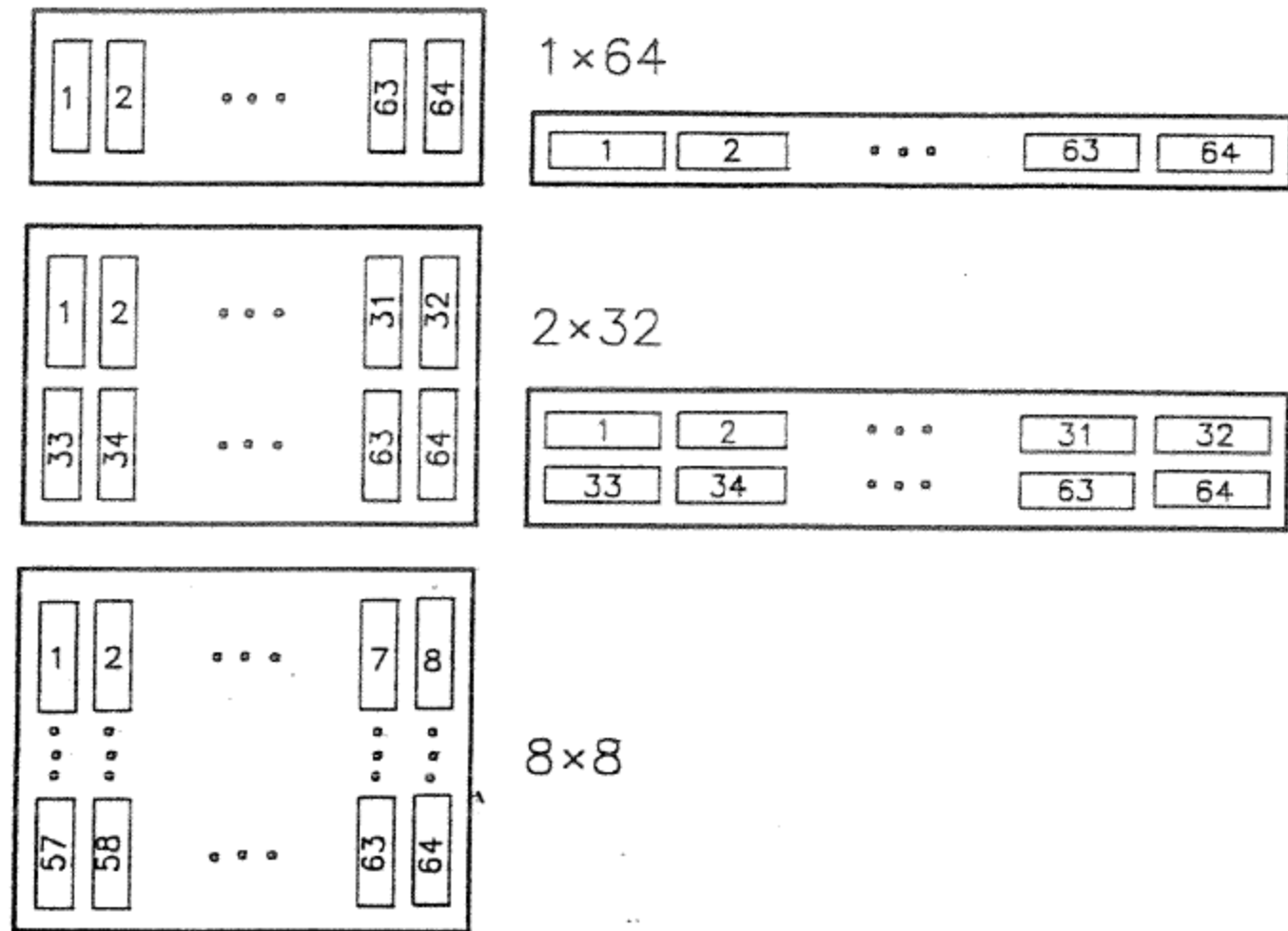Fig. 2. A layout derived from the floorplan in Fig. 1

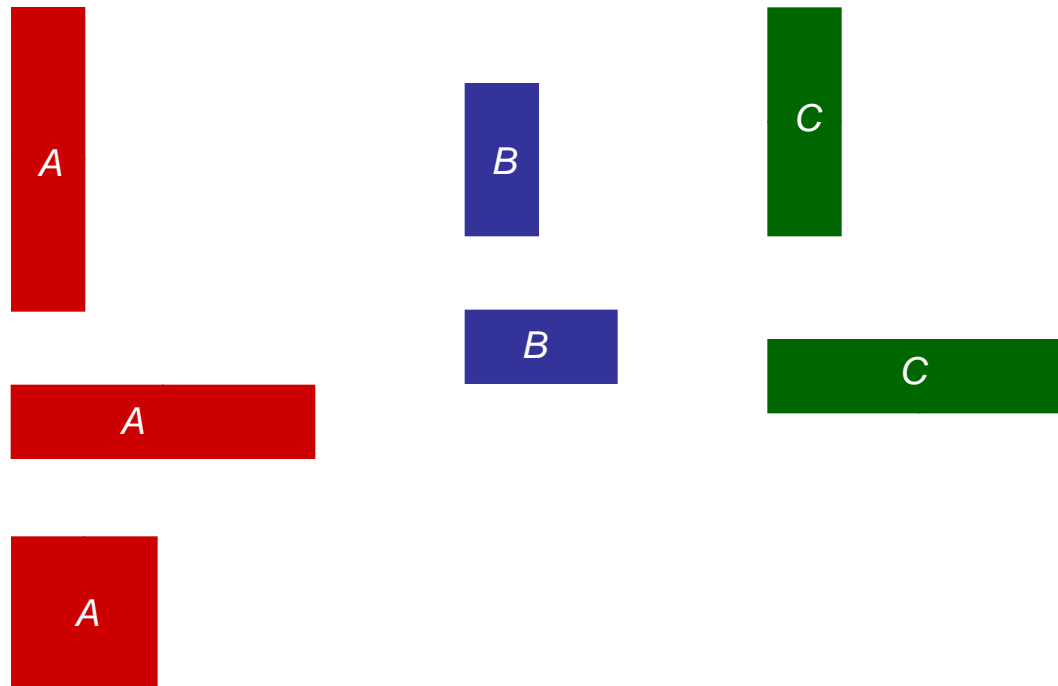Figure 3. Some possible implementations of a register file.

Example

Given: Three blocks with the following potential widths and heights

Block *A*: $w = 1$, $h = 4$ or $w = 4$, $h = 1$ or $w = 2$, $h = 2$

Block *B*: $w = 1$, $h = 2$ or $w = 2$, $h = 1$

Block *C*: $w = 1$, $h = 3$ or $w = 3$, $h = 1$

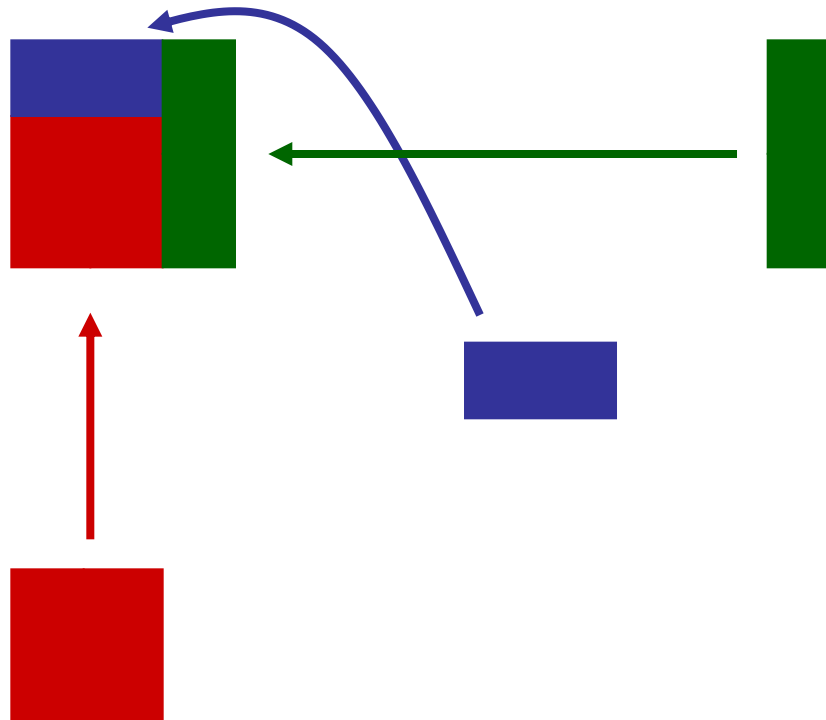Task: Floorplan with minimum total area enclosed

Example
Given: Three blocks with the following potential widths and heights
Block A: $w = 1$, $h = 4$ or $w = 4$, $h = 1$ or $w = 2$, $h = 2$
Block B: $w = 1$, $h = 2$ or $w = 2$, $h = 1$
Block C: $w = 1$, $h = 3$ or $w = 3$, $h = 1$

Task: Floorplan with minimum total area enclosed

Example

Given: Three blocks with the following potential widths and heights

Block A: $w = 1, h = 4$ or $w = 4, h = 1$ or $w = 2, h = 2$

Block B: $w = 1, h = 2$ or $w = 2, h = 1$

Block C: $w = 1, h = 3$ or $w = 3, h = 1$

Task: Floorplan with minimum total area enclosed

Solution:

Aspect ratios

Block A with $w = 2, h = 2$; Block B with $w = 2, h = 1$; Block C with $w = 1, h = 3$

This floorplan has a global bounding box with minimum possible area (9 square units).

- Area and shape of the global bounding box
  - Global bounding box of a floorplan is the minimum axis-aligned rectangle that contains all floorplan blocks.
  - Area of the global bounding box represents the area of the top-level floorplan
  - Minimizing the area involves by finding the shapes of the individual blocks.

- A rectangular dissection is a division of the chip area into a set of *blocks* or non-overlapping rectangles.

- A slicing floorplan is a rectangular dissection
  - Obtained by repeatedly dividing each rectangle, starting with the entire chip area, into two smaller rectangles
  - Horizontal or vertical cut line.

- A slicing tree or slicing floorplan tree is a binary tree with k leaves and $k - 1$ internal nodes
  - Each leaf represents a block
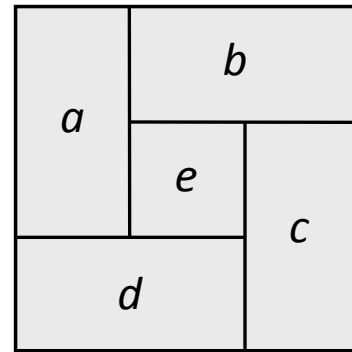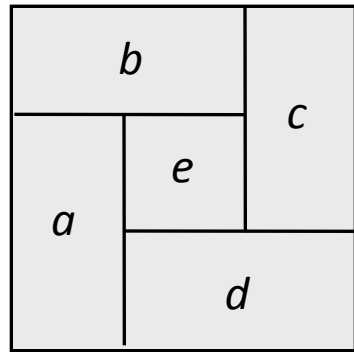 - Each internal node represents a horizontal or vertical cut line.

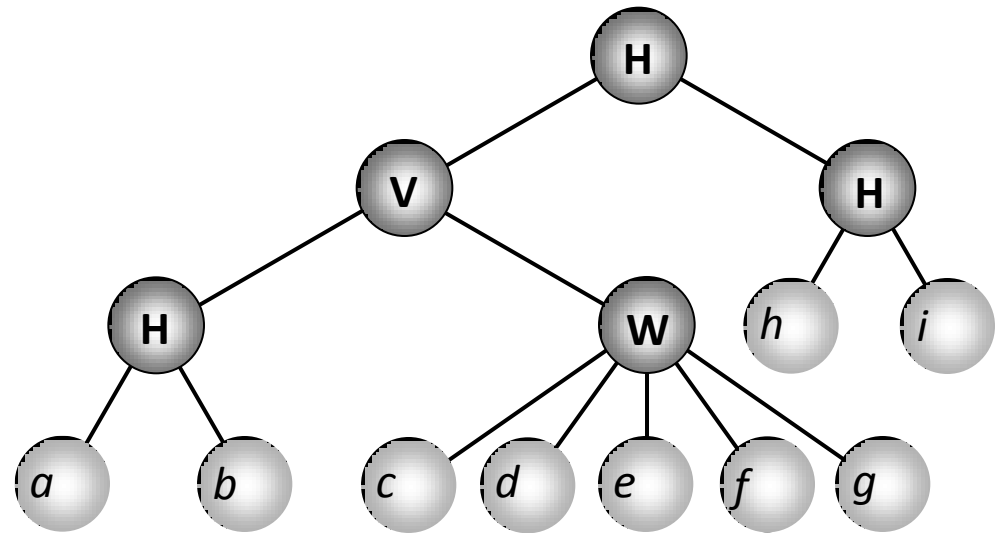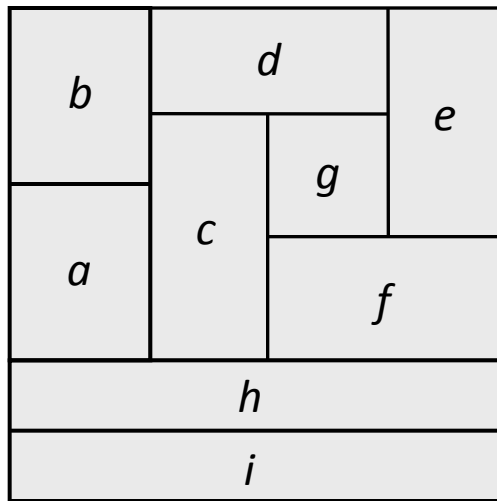# Slicing floorplan and corresponding slicing trees
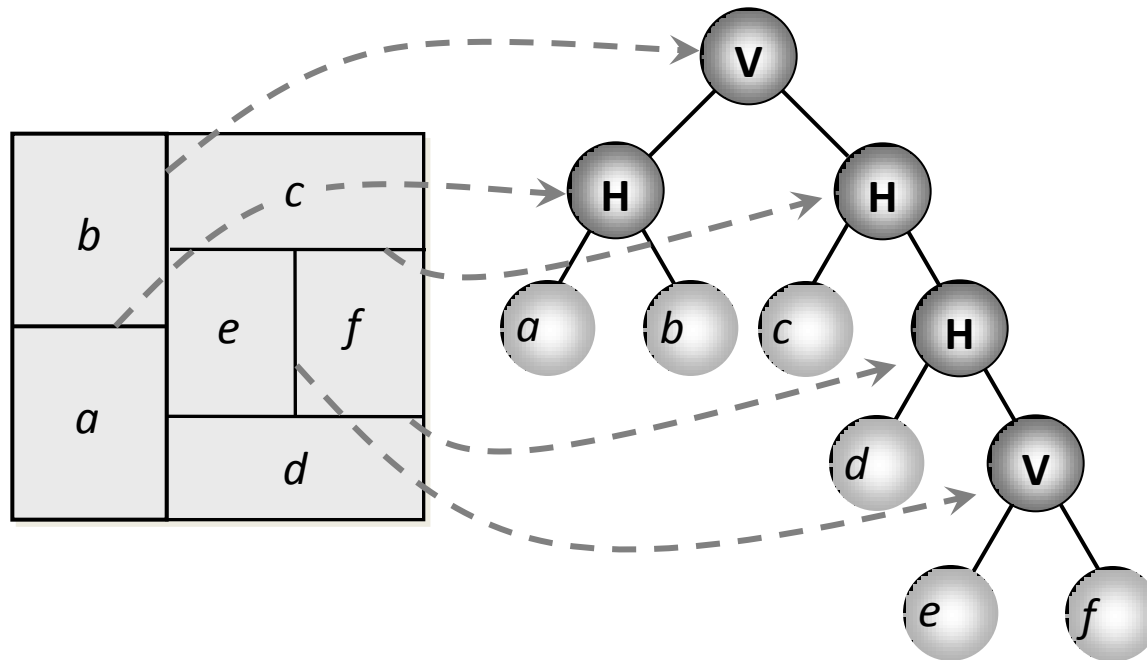
Non-slicing floorplans (wheels)

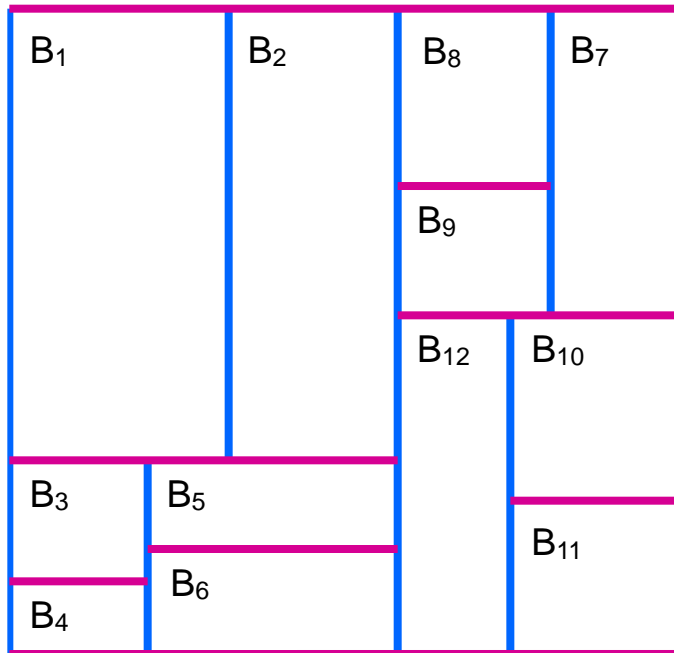# Floorplan tree: Tree that represents a hierarchical floorplan

H — Horizontal division
(objects to the top and bottom)

V — Vertical division
(objects to the left and right)

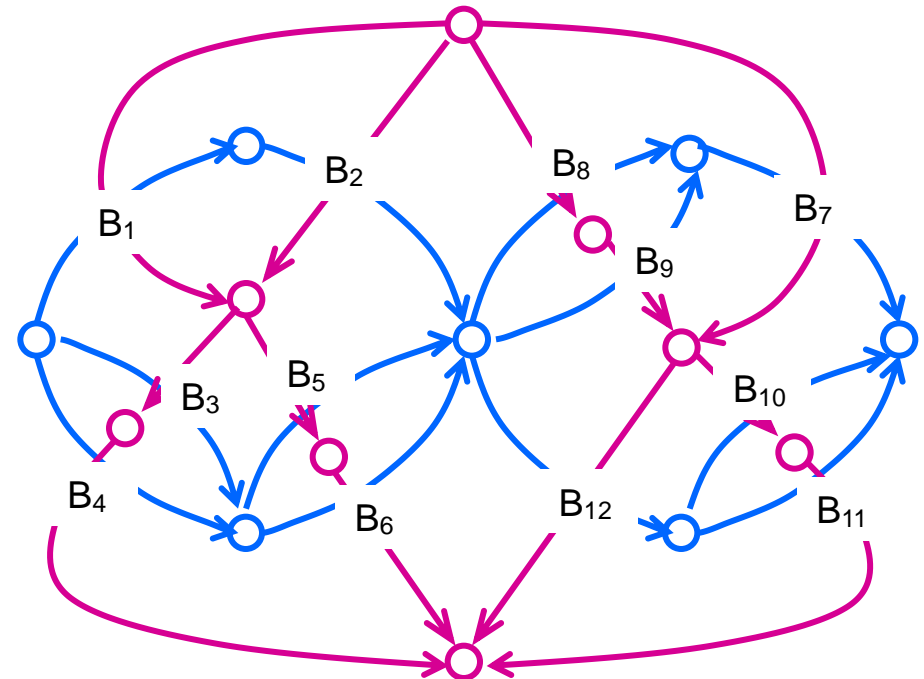W — Wheel (4 objects cycled around a center object)

Floorplan and Layout

Floorplan

Graph representation

Floorplan is represented by a planar graph.

Vertices - vertical lines. Arcs - rectangular areas where blocks are embedded.

A dual graph is implied.

From Floorplan to Layout

- Actual layout is obtained by embedding real blocks into floorplan cells.

  - Blocks' adjacency relations are maintained

  - Blocks are not perfectly matched, thus white area (waste) results

- Layout width and height are obtained by assigning blocks' dimensions to corresponding arcs.

  - Width and height are derived from longest paths

- Different block sizes yield different layout area, even if block sizes are area invariant.